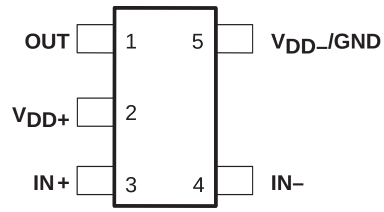
- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 21 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Very Low Power . . . 11 μA Per Channel Typ**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **Wide Supply Voltage Range 2.7 V to 10 V**
- **Available in the SOT-23 Package**
- **Macromodel Included**

**DBV PACKAGE**
**(TOP VIEW)**

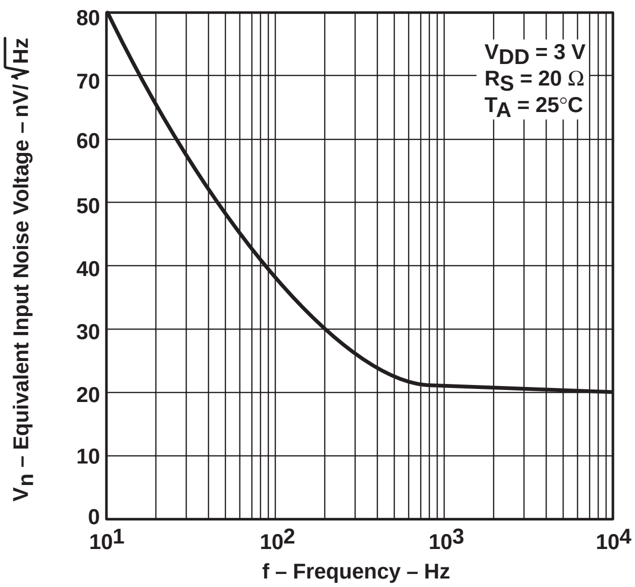



## description

The TLV2711 is a single low-voltage operational amplifier available in the SOT-23 package. It consumes only 11 μA (typ) of supply current and is ideal for battery-power applications. Looking at Figure 1, the TLV2711 has a 3-V noise level of 21 nV/√Hz at 1 kHz; five times lower than competitive SOT-23 micropower solutions. The device exhibits rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLV2711 is fully characterized at 3 V and 5 V and is optimized for low-voltage applications.

The TLV2711, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micro-power dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs).

**EQUIVALENT INPUT NOISE VOLTAGE†**
**vs**
**FREQUENCY**




† For all curves where $V_{DD}$ = 5 V, all loads are referenced to 2.5 V.
For all curves where $V_{DD}$ = 3 V, all loads are referenced to 1.5 V.

**Figure 1. Equivalent Input Noise Voltage Versus Frequency**

With a total area of 5.6mm$^2$, the SOT-23 package only requires one-third the board space of the standard 8-pin SOIC package. This ultra-small package allows designers to place single amplifiers very close to the signal source, minimizing noise pick-up from long PCB traces.

**AVAILABLE OPTIONS**

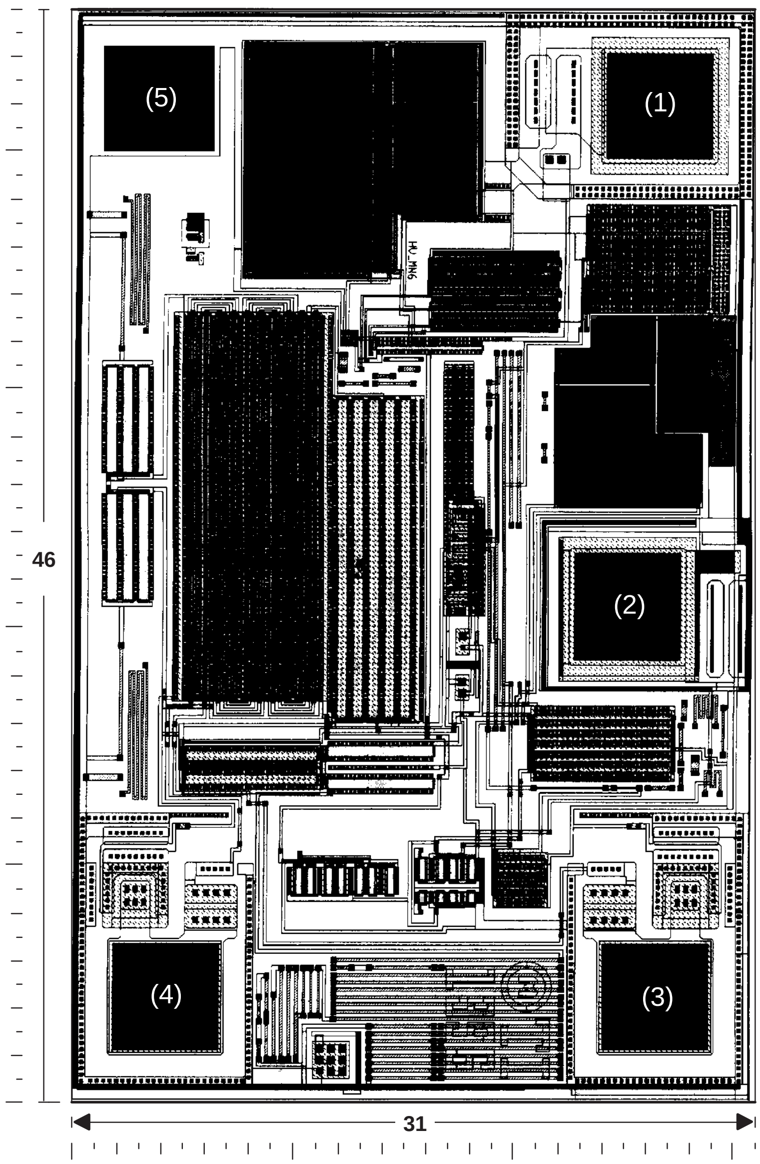
| $T_A$ | $V_{IO}$max AT 25°C | PACKAGED DEVICES SOT-23 (DBV)† | SYMBOL | CHIP FORM‡ (Y) |
|---|---|---|---|---|
| 0°C to 70°C | 3 mV | TLV2711CDBV | VAJC | TLV2711Y |
| –40°C to 85°C | 3 mV | TLV2711IDBV | VAJI | |

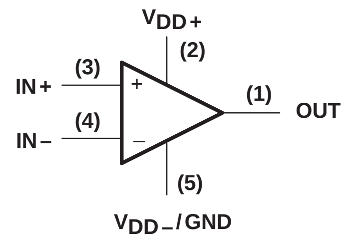
† The DBV package available in tape and reel only.
‡ Chip forms are tested at $T_A$ = 25°C only.

## TLV2711Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2711C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS




CHIP THICKNESS: 10 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

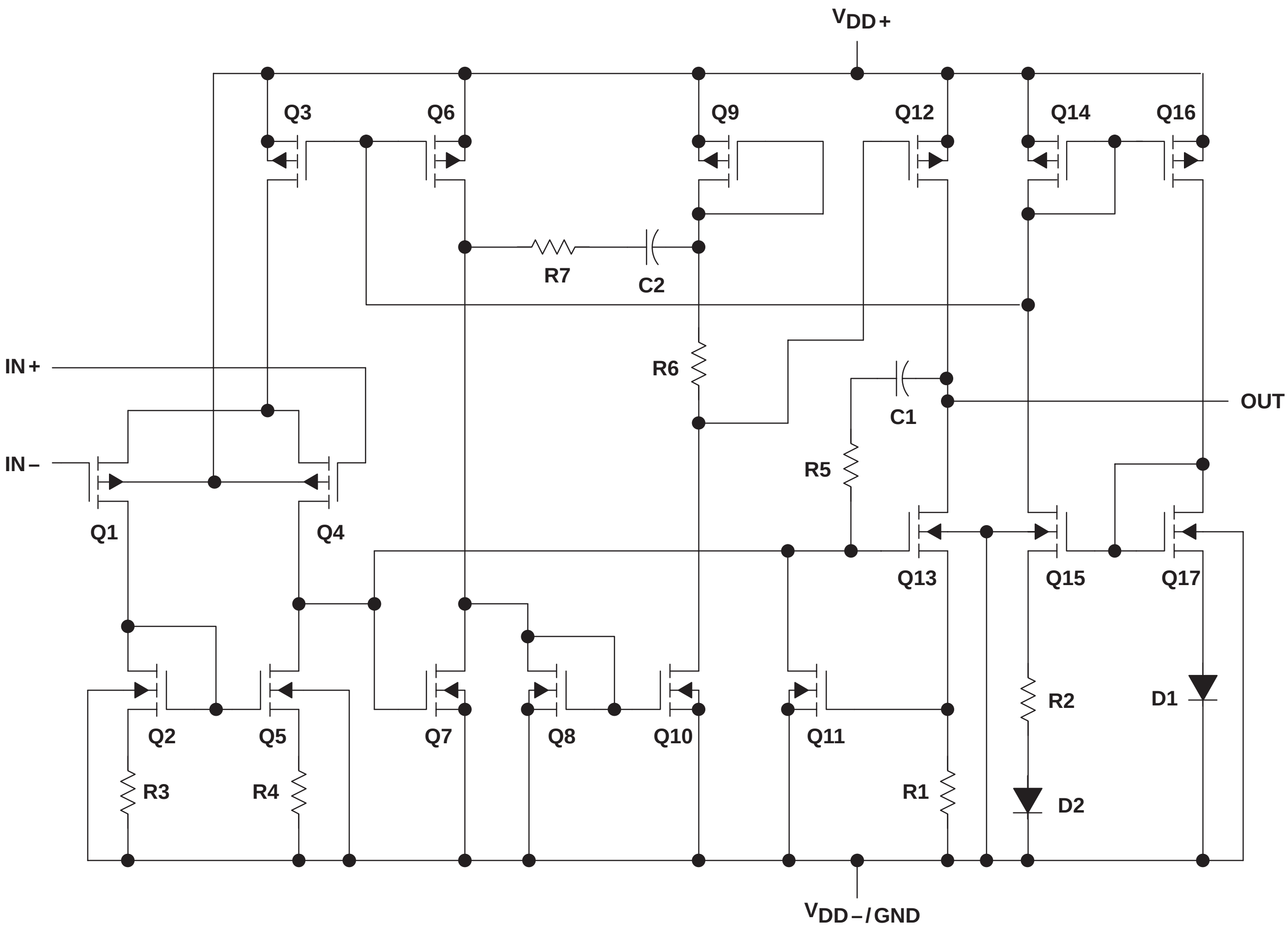
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (2) IS INTERNALLY CONNECTED TO BACK SIDE OF CHIP.

## equivalent schematic




| COMPONENT COUNT† | |
|---|---|
| Transistors | 23 |
| Diodes | 6 |
| Resistors | 11 |
| Capacitors | 2 |

† Includes both amplifiers and all ESD, bias, and trim circuitry

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{DD}$ (see Note 1) . . . 12 V
Differential input voltage, $V_{ID}$ (see Note 2) . . . $\pm V_{DD}$
Input voltage range, $V_I$ (any input, see Note 1) . . . –0.3 V to $V_{DD}$
Input current, $I_I$ (each input) . . . ±5 mA
Output current, $I_O$ . . . ±50 mA
Total current into $V_{DD+}$ . . . ±50 mA
Total current out of $V_{DD-}$ . . . ±50 mA
Duration of short-circuit current (at or below) 25°C (see Note 3) . . . unlimited
Continuous total power dissipation . . . See Dissipation Rating Table
Operating free-air temperature range, $T_A$: TLV2711C . . . 0°C to 70°C
TLV2711I . . . –40°C to 85°C
Storage temperature range, $T_{stg}$ . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DBV package . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to $V_{DD-}$.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought below $V_{DD-}$ – 0.3 V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \leq 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A$ = 25°C | $T_A$ = 70°C POWER RATING | $T_A$ = 85°C POWER RATING |
|---|---|---|---|---|
| DBV | 150 mW | 1.2 mW/°C | 96 mW | 78 mW |

## recommended operating conditions

| | TLV2711C | | TLV2711I | | UNIT |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| Supply voltage, $V_{DD}$ (see Note 1) | 2.7 | 10 | 2.7 | 10 | V |
| Input voltage range, $V_I$ | $V_{DD-}$ | $V_{DD+}$ –1.3 | $V_{DD-}$ | $V_{DD+}$ –1.3 | V |
| Common-mode input voltage, $V_{IC}$ | $V_{DD-}$ | $V_{DD+}$ –1.3 | $V_{DD-}$ | $V_{DD+}$ –1.3 | V |
| Operating free-air temperature, $T_A$ | 0 | 70 | –40 | 85 | °C |

NOTE 1: All voltage values, except differential voltages, are with respect to $V_{DD-}$.

## electrical characteristics at specified free-air temperature, $V_{DD}$ = 3 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$† | TLV2711C MIN | TLV2711C TYP | TLV2711C MAX | TLV2711I MIN | TLV2711I TYP | TLV2711I MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IO}$ | Input offset voltage | $V_{DD\pm}$ = ±1.5 V, $V_{IC}$ = 0, $V_O$ = 0, $R_S$ = 50 Ω | Full range | | 0.4 | 3 | | 0.4 | 3 | mV |
| $\alpha_{VIO}$ | Temperature coefficient of input offset voltage | | Full range | | 1 | | | 1 | | µV/°C |
| | Input offset voltage long-term drift (see Note 4) | | 25°C | | 0.003 | | | 0.003 | | µV/mo |
| $I_{IO}$ | Input offset current | | 25°C | | 0.5 | 60 | | 0.5 | 60 | pA |
| | | | Full range | | | 150 | | | 150 | |
| $I_{IB}$ | Input bias current | | 25°C | | | 60 | | | 60 | |
| | | | Full range | | 1 | 150 | | 1 | 150 | |
| $V_{ICR}$ | Common-mode input voltage range | $\|V_{IO}\| \le 5$ mV, $R_S$ = 50 Ω | 25°C | 0 to 2 | –0.3 to 2.2 | | 0 to 2 | –0.3 to 2.2 | | V |
| | | | Full range | 0 to 1.7 | | | 0 to 1.7 | | | |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –100 µA | 25°C | | 2.94 | | | 2.94 | | V |
| | | $I_{OH}$ = –250 µA | 25°C | | 2.85 | | | 2.85 | | |
| | | | Full range | 2.6 | | | 2.6 | | | |
| $V_{OL}$ | Low-level output voltage | $V_{IC}$ = 1.5 V, $I_{OL}$ = 50 µA | 25°C | | 15 | | | 15 | | mV |
| | | $V_{IC}$ = 1.5 V, $I_{OL}$ = 500 µA | 25°C | | 150 | | | 150 | | |
| | | | Full range | | | 500 | | | 500 | |
| $A_{VD}$ | Large-signal differential voltage amplification | $V_{IC}$ = 1.5 V, $V_O$ = 1 V to 2 V, $R_L$ = 10 kΩ‡ | 25°C | 3 | 7 | | 3 | 7 | | V/mV |
| | | | Full range | 1 | | | 1 | | | |
| | | $V_{IC}$ = 1.5 V, $V_O$ = 1 V to 2 V, $R_L$ = 1 MΩ‡ | 25°C | | 600 | | | 600 | | |
| $r_{i(d)}$ | Differential input resistance | | 25°C | | $10^{12}$ | | | $10^{12}$ | | Ω |
| $r_{i(c)}$ | Common-mode input resistance | | 25°C | | $10^{12}$ | | | $10^{12}$ | | Ω |
| $c_{i(c)}$ | Common-mode input capacitance | f = 10 kHz, | 25°C | | 5 | | | 5 | | pF |
| $z_o$ | Closed-loop output impedance | f = 7 kHz, $A_V$ = 1 | 25°C | | 200 | | | 200 | | Ω |
| CMRR | Common-mode rejection ratio | $V_{IC}$ = 0 to 1.7 V, $V_O$ = 1.5 V, $R_S$ = 50 Ω | 25°C | 65 | 83 | | 65 | 83 | | dB |
| | | | Full range | 60 | | | 60 | | | |
| $k_{SVR}$ | Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$) | $V_{DD}$ = 2.7 V to 8 V, $V_{IC}$ = $V_{DD}$/2 , No load | 25°C | 80 | 95 | | 80 | 95 | | dB |
| | | | Full range | 80 | | | 80 | | | |
| $I_{DD}$ | Supply current | $V_O$ = 1.5 V, No load | 25°C | | 11 | 25 | | 11 | 25 | µA |
| | | | Full range | | | 30 | | | 30 | |

† Full range for the TLV2711C is 0°C to 70°C. Full range for the TLV2711I is – 40°C to 85°C.
‡ Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A$ = 150°C extrapolated to $T_A$ = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

## operating characteristics at specified free-air temperature, $V_{DD}$ = 3 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$† | TLV2711C | | | TLV2711I | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| SR | Slew rate at unity gain | $V_O$ = 1.1 V to 1.9 V, $R_L$ = 10 kΩ‡, $C_L$ = 100 pF‡ | 25°C | 0.01 | 0.025 | | 0.01 | 0.025 | | V/μs |
| | | | Full range | 0.005 | | | 0.005 | | | |
| $V_n$ | Equivalent input noise voltage | f = 10 Hz | 25°C | | 80 | | | 80 | | nV/√Hz |
| | | f = 1 kHz | 25°C | | 22 | | | 22 | | |
| $V_{N(PP)}$ | Peak-to-peak equivalent input noise voltage | f = 0.1 Hz to 1 Hz | 25°C | | 660 | | | 660 | | nV |
| | | f = 0.1 Hz to 10 Hz | 25°C | | 880 | | | 880 | | |
| $I_n$ | Equivalent input noise current | | 25°C | | 0.6 | | | 0.6 | | fA /√Hz |
| | Gain-bandwidth product | f = 10 kHz, $R_L$ = 10 kΩ‡, $C_L$ = 100 pF‡ | 25°C | | 56 | | | 56 | | kHz |
| $B_{OM}$ | Maximum output-swing bandwidth | $V_{O(PP)}$ = 1 V, $A_V$ = 1, $R_L$ = 10 kΩ‡, $C_L$ = 100 pF‡ | 25°C | | 7 | | | 7 | | kHz |
| $\phi_m$ | Phase margin at unity gain | $R_L$ = 10 kΩ‡, $C_L$ = 100 pF‡ | 25°C | | 56° | | | 56° | | |
| | Gain margin | | 25°C | | 20 | | | 20 | | dB |

† Full range is –40°C to 85°C.
‡ Referenced to 1.5 V

## electrical characteristics at specified free-air temperature, $V_{DD}$ = 5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$† | TLV2711C MIN | TLV2711C TYP | TLV2711C MAX | TLV2711I MIN | TLV2711I TYP | TLV2711I MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IO}$ | Input offset voltage | $V_{DD\pm}$ = ±2.5 V, $V_{IC}$ = 0, $V_O$ = 0, $R_S$ = 50 Ω | Full range | | 0.45 | 3 | | 0.45 | 3 | mV |
| $\alpha_{VIO}$ | Temperature coefficient of input offset voltage | | Full range | | 0.5 | | | 0.5 | | µV/°C |
| | Input offset voltage long-term drift (see Note 4) | | 25°C | | 0.003 | | | 0.003 | | µV/mo |
| $I_{IO}$ | Input offset current | | 25°C | | 0.5 | 60 | | 0.5 | 60 | pA |
| | | | Full range | | | 150 | | | 150 | |
| $I_{IB}$ | Input bias current | | 25°C | | 1 | 60 | | 1 | 60 | pA |
| | | | Full range | | | 150 | | | 150 | |
| $V_{ICR}$ | Common-mode input voltage range | $\|V_{IO}\| \le$ 5 mV, $R_S$ = 50 Ω | 25°C | 0 to 4 | −0.3 to 4.2 | | 0 to 4 | −0.3 to 4.2 | | V |
| | | | Full range | 0 to 3.5 | | | 0 to 3.5 | | | |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = −100 µA | 25°C | | 4.95 | | | 4.95 | | V |
| | | $I_{OH}$ = −250 µA | 25°C | | 4.875 | | | 4.875 | | |
| | | | Full range | 4.6 | | | 4.6 | | | |
| $V_{OL}$ | Low-level output voltage | $V_{IC}$ = 2.5 V, $I_{OL}$ = 50 µA | 25°C | | 12 | | | 12 | | mV |
| | | $V_{IC}$ = 2.5 V, $I_{OL}$ = 500 µA | 25°C | | 120 | | | 120 | | |
| | | | Full range | | | 500 | | | 500 | |
| $A_{VD}$ | Large-signal differential voltage amplification | $V_{IC}$ = 2.5 V, $V_O$ = 1 V to 4 V, $R_L$ = 10 kΩ‡ | 25°C | 6 | 12 | | 6 | 12 | | V/mV |
| | | | Full range | 3 | | | 3 | | | |
| | | $V_{IC}$ = 2.5 V, $V_O$ = 1 V to 4 V, $R_L$ = 1 MΩ‡ | 25°C | | 800 | | | 800 | | |
| $r_{i(d)}$ | Differential input resistance | | 25°C | | $10^{12}$ | | | $10^{12}$ | | Ω |
| $r_{i(c)}$ | Common-mode input resistance | | 25°C | | $10^{12}$ | | | $10^{12}$ | | Ω |
| $c_{i(c)}$ | Common-mode input capacitance | f = 10 kHz, | 25°C | | 5 | | | 5 | | pF |
| $z_o$ | Closed-loop output impedance | f = 7 kHz, $A_V$ = 1 | 25°C | | 200 | | | 200 | | Ω |
| CMRR | Common-mode rejection ratio | $V_{IC}$ = 0 to 2.7 V, $V_O$ = 2.5 V, $R_S$ = 50 Ω | 25°C | 70 | 83 | | 70 | 83 | | dB |
| | | | Full range | 70 | | | 70 | | | |
| $k_{SVR}$ | Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$) | $V_{DD}$ = 4.4 V to 8 V, $V_{IC} = V_{DD}/2$, No load | 25°C | 80 | 95 | | 80 | 95 | | dB |
| | | | Full range | 80 | | | 80 | | | |
| $I_{DD}$ | Supply current | $V_O$ = 2.5 V, No load | 25°C | | 13 | 25 | | 13 | 25 | µA |
| | | | Full range | | | 30 | | | 30 | |

† Full range for the TLV2711C is 0°C to 70°C. Full range for the TLV2711I is – 40°C to 85°C.
‡ Referenced to 1.5 V

NOTE 5: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A$ = 150°C extrapolated to $T_A$ = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

## operating characteristics at specified free-air temperature, $V_{DD}$ = 5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$† | TLV2711C | | | TLV2711I | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| SR | Slew rate at unity gain | $V_O$ = 1.5 V to 3.5 V, $R_L$ = 10 kΩ‡, $C_L$ = 100 pF‡ | 25°C | 0.01 | 0.025 | | 0.01 | 0.025 | | V/μs |
| | | | Full range | 0.005 | | | 0.005 | | | |
| $V_n$ | Equivalent input noise voltage | f = 10 Hz | 25°C | | 72 | | | 72 | | nV/√Hz |
| | | f = 1 kHz | 25°C | | 21 | | | 21 | | |
| $V_{N(PP)}$ | Peak-to-peak equivalent input noise voltage | f = 0.1 Hz to 1 Hz | 25°C | | 600 | | | 600 | | nV |
| | | f = 0.1 Hz to 10 Hz | 25°C | | 800 | | | 800 | | |
| $I_n$ | Equivalent input noise current | | 25°C | | 0.6 | | | 0.6 | | fA/√Hz |
| | Gain-bandwidth product | f = 10 kHz, $R_L$ = 10 kΩ‡, $C_L$ = 100 pF‡ | 25°C | | 65 | | | 65 | | kHz |
| $B_{OM}$ | Maximum output-swing bandwidth | $V_{O(PP)}$ = 2 V, $A_V$ = 1, $R_L$ = 10 kΩ‡, $C_L$ = 100 pF‡ | 25°C | | 7 | | | 7 | | kHz |
| $\phi_m$ | Phase margin at unity gain | $R_L$ = 10 kΩ‡, $C_L$ = 100 pF‡ | 25°C | | 60° | | | 60° | | |
| | Gain margin | | 25°C | | 22 | | | 22 | | dB |

† Full range is –40°C to 85°C.
‡ Referenced to 1.5 V

## electrical characteristics at $V_{DD}$ = 3 V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TLV2711Y | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| $V_{IO}$ | Input offset voltage | $V_{DD\pm}$ = ±1.5 V, $V_O$ = 0, $V_{IC}$ = 0, $R_S$ = 50 Ω | | 0.47 | | mV |
| $I_{IO}$ | Input offset current | | | 0.5 | | pA |
| $I_{IB}$ | Input bias current | | | 1 | | pA |
| $V_{ICR}$ | Common-mode input voltage range | $\lvert V_{IO} \rvert$ ≤5 mV, $R_S$ = 50 Ω | | –0.3 to 2.2 | | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –100 μA | | 2.94 | | V |
| | | $I_{OH}$ = –200 μA | | 2.85 | | |
| $V_{OL}$ | Low-level output voltage | $V_{IC}$ = 0, $I_{OL}$ = 50 μA | | 15 | | mV |
| | | $V_{IC}$ = 0, $I_{OL}$ = 500 μA | | 150 | | |
| $A_{VD}$ | Large-signal differential voltage amplification | $V_{IC}$ = 1.5 V, $V_O$ = 1 V to 2 V, $R_L$ = 10 kΩ† | | 7 | | V/mV |
| | | $V_{IC}$ = 1.5 V, $V_O$ = 1 V to 2 V, $R_L$ = 1 MΩ† | | 600 | | |
| $r_{i(d)}$ | Differential input resistance | | | $10^{12}$ | | Ω |
| $r_{i(c)}$ | Common-mode input resistance | | | $10^{12}$ | | Ω |
| $c_{i(c)}$ | Common-mode input capacitance | f = 10 kHz | | 5 | | pF |
| $z_o$ | Closed-loop output impedance | f = 7 kHz, $A_V$ = 1 | | 200 | | Ω |
| CMRR | Common-mode rejection ratio | $V_{IC}$ = 0 to 1.7 V, $V_O$ = 1.5 V, $R_S$ = 50 Ω | | 83 | | dB |
| $k_{SVR}$ | Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$) | $V_{DD}$ = 2.7 V to 8 V, $V_{IC}$ = $V_{DD}$/2, No load | | 95 | | dB |
| $I_{DD}$ | Supply current | $V_O$ = 1.5 V, No load | | 11 | | μA |

† Referenced to 1.5 V

## electrical characteristics at $V_{DD}$ = 5 V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | TLV2711Y MIN | TLV2711Y TYP | TLV2711Y MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IO}$ | Input offset voltage | $V_{DD}\pm = \pm2.5$ V, $R_S$ = 50 Ω | $V_{IC}$ = 0, | $V_O$ = 0, | | 0.45 | | mV |
| $I_{IO}$ | Input offset current | | | | | 0.5 | | pA |
| $I_{IB}$ | Input bias current | | | | | 1 | | pA |
| $V_{ICR}$ | Common-mode input voltage range | $\lvert V_{IO} \rvert \le 5$ mV, | $R_S$ = 50 Ω | | | –0.3 to 4.2 | | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –100 µA | | | | 4.95 | | V |
| | | $I_{OH}$ = –250 µA | | | | 4.875 | | |
| $V_{OL}$ | Low-level output voltage | $V_{IC}$ = 2.5 V, | $I_{OL}$ = 50 µA | | | 12 | | mV |
| | | $V_{IC}$ = 2.5 V, | $I_{OL}$ = 500 µA | | | 120 | | |
| $A_{VD}$ | Large-signal differential voltage amplification | $V_{IC}$ = 2.5 V, | $V_O$ = 1 V to 4 V | $R_L$ = 10 kΩ† | | 12 | | V/mV |
| | | | | $R_L$ = 1 MΩ† | | 800 | | |
| $r_{i(d)}$ | Differential input resistance | | | | | $10^{12}$ | | Ω |
| $r_{i(c)}$ | Common-mode input resistance | | | | | $10^{12}$ | | Ω |
| $c_{i(c)}$ | Common-mode input capacitance | f = 10 kHz | | | | 5 | | pF |
| $z_o$ | Closed-loop output impedance | f = 7 kHz, | $A_V$ = 1 | | | 200 | | Ω |
| CMRR | Common-mode rejection ratio | $V_{IC}$ = 0 to 2.7 V, | $V_O$ = 2.5 V, | $R_S$ = 50 Ω | | 83 | | dB |
| $k_{SVR}$ | Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$) | $V_{DD}$ = 4.4 V to 8 V, | $V_{IC} = V_{DD}/2$, | No load | | 95 | | dB |
| $I_{DD}$ | Supply current | $V_O$ = 2.5 V, | No load | | | 13 | | µA |

† Referenced to 1.5 V

## TYPICAL CHARACTERISTICS

### Table of Graphs

| | | | FIGURE |
|---|---|---|---|
| $V_{IO}$ | Input offset voltage | Distribution<br>vs Common-mode input voltage | 2, 3<br>4, 5 |
| $\alpha_{VIO}$ | Input offset voltage temperature coefficient | Distribution | 6, 7 |
| $I_{IB}/I_{IO}$ | Input bias and input offset currents | vs Free-air temperature | 8 |
| $V_I$ | Input voltage | vs Supply voltage<br>vs Free-air temperature | 9<br>10 |
| $V_{OH}$ | High-level output voltage | vs High-level output current | 11, 14 |
| $V_{OL}$ | Low-level output voltage | vs Low-level output current | 12, 13, 15 |
| $V_{O(PP)}$ | Maximum peak-to-peak output voltage | vs Frequency | 16 |
| $I_{OS}$ | Short-circuit output current | vs Supply voltage<br>vs Free-air temperature | 17<br>18 |
| $V_O$ | Output voltage | vs Differential input voltage | 19, 20 |
| $A_{VD}$ | Large-signal differential voltage amplification and phase margin | vs Load resistance<br>vs Frequency<br>vs Free-air temperature | 21<br>22, 23<br>24, 25 |
| $z_o$ | Output impedance | vs Frequency | 26, 27 |
| CMRR | Common-mode rejection ratio | vs Frequency<br>vs Free-air temperature | 28<br>29 |
| $k_{SVR}$ | Supply-voltage rejection ratio | vs Frequency<br>vs Free-air temperature | 30, 31<br>32 |
| $I_{DD}$ | Supply current | vs Supply voltage | 33 |
| SR | Slew rate | vs Load capacitance<br>vs Free-air temperature | 34<br>35 |
| $V_O$ | Large-signal pulse response | vs Time | 36, 37, 38, 39 |
| | Inverting small-signal pulse response | | 40, 41 |
| | Small-signal pulse response | | 42, 43 |
| $V_n$ | Equivalent input noise voltage | vs Frequency | 44, 45 |
| | Noise voltage (referred to input) | Over a 10-second period | 46 |
| THD + N | Total harmonic distortion plus noise | vs Frequency | 47 |
| | Gain-bandwidth product | vs Free-air temperature<br>vs Supply voltage | 48<br>49 |
| $\phi_m$ | Phase margin | vs Frequency<br>vs Load capacitance | 23, 24<br>50 |
| | Gain margin | vs Load capacitance | 51 |
| $B_1$ | Unity-gain bandwidth | vs Load capacitance | 52 |

## TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLV2711 INPUT OFFSET VOLTAGE**

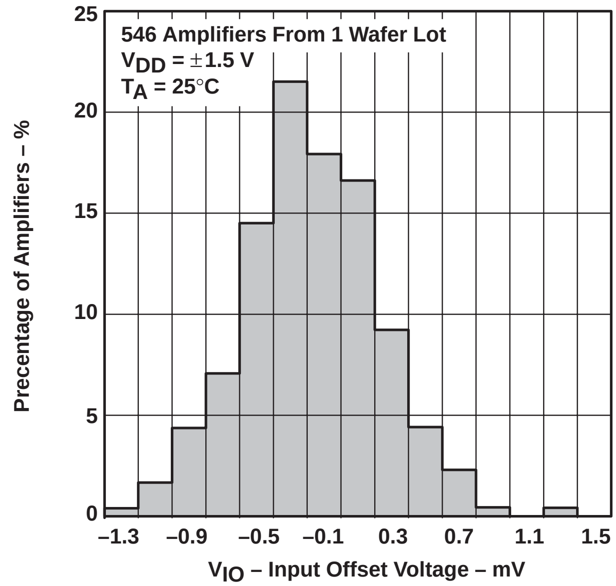



Figure 2

**DISTRIBUTION OF TLV2711 INPUT OFFSET VOLTAGE**

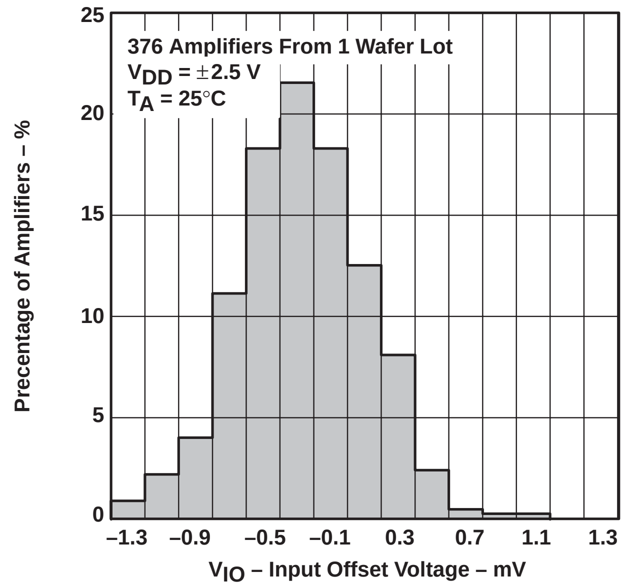



Figure 3

**INPUT OFFSET VOLTAGE† vs COMMON-MODE INPUT VOLTAGE**

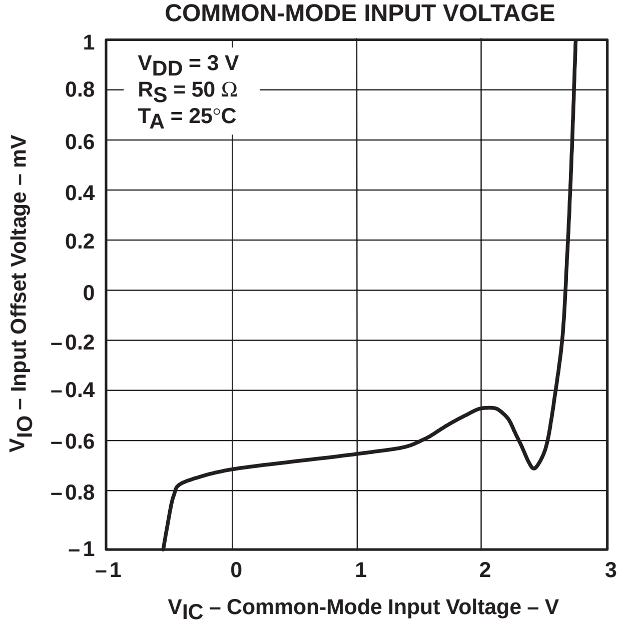



Figure 4

**INPUT OFFSET VOLTAGE† vs COMMON-MODE INPUT VOLTAGE**

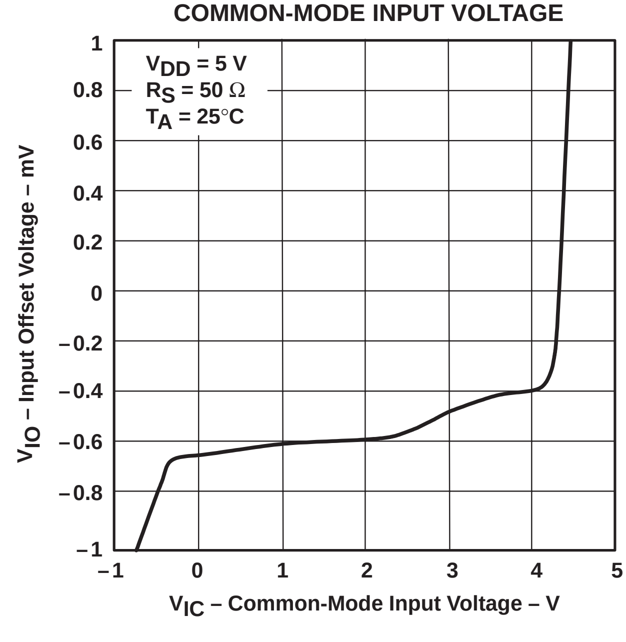



Figure 5

† For all curves where $V_{DD}$ = 5 V, all loads are referenced to 2.5 V. For all curves where $V_{DD}$ = 3 V, all loads are referenced to 1.5 V.

## TYPICAL CHARACTERISTICS

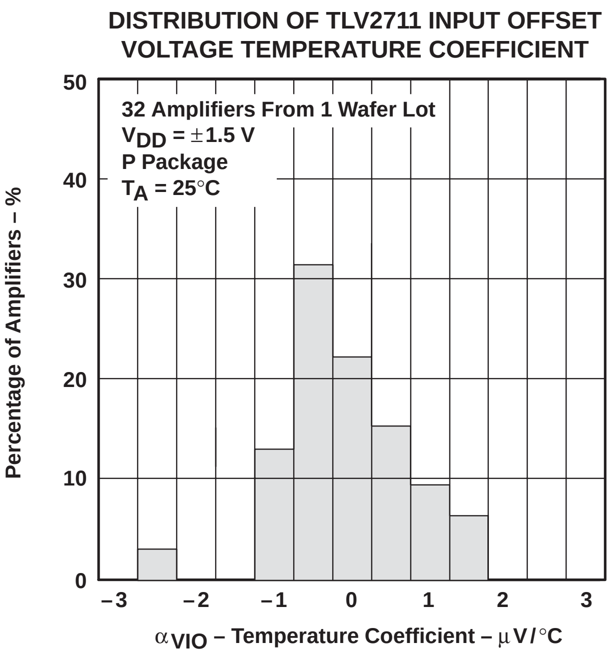



Figure 6

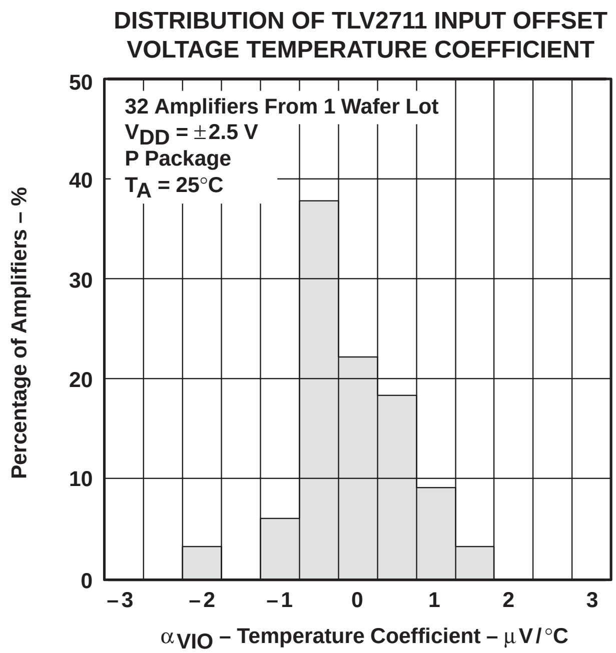



Figure 7

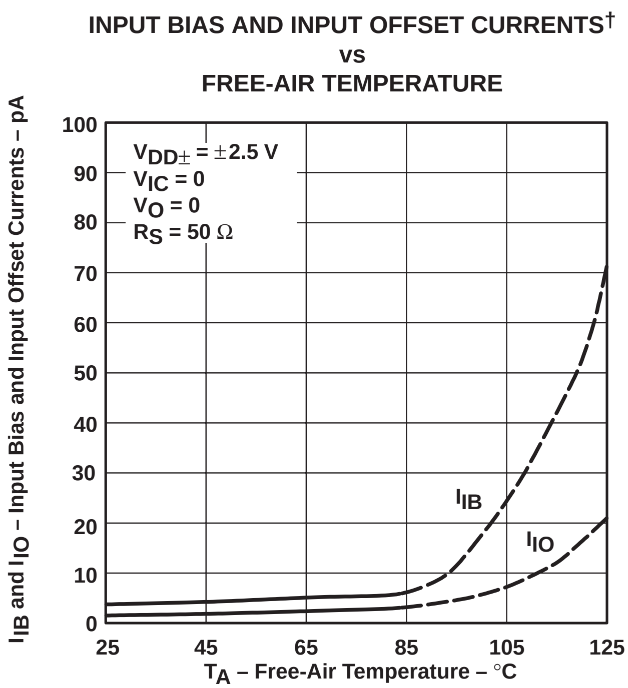



Figure 8

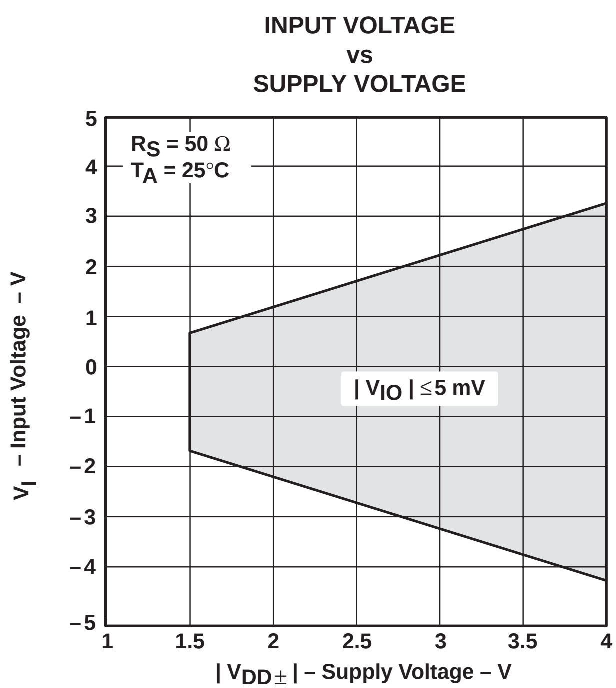



Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

## TYPICAL CHARACTERISTICS

**INPUT VOLTAGE†‡ vs FREE-AIR TEMPERATURE**

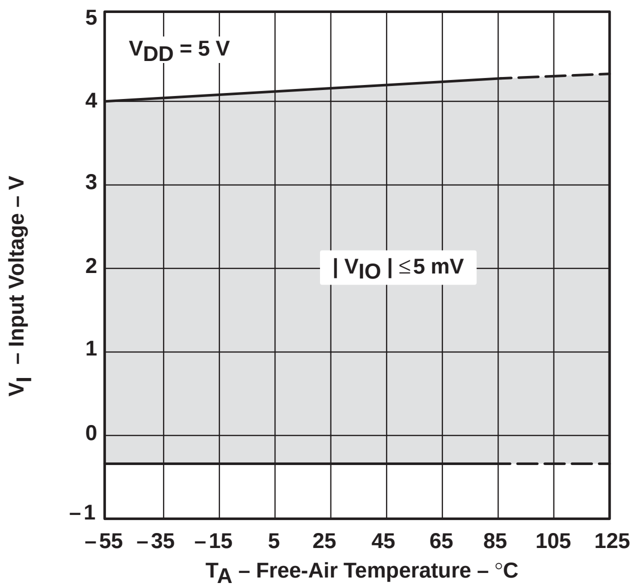



Figure 10

**HIGH-LEVEL OUTPUT VOLTAGE†‡ vs HIGH-LEVEL OUTPUT CURRENT**

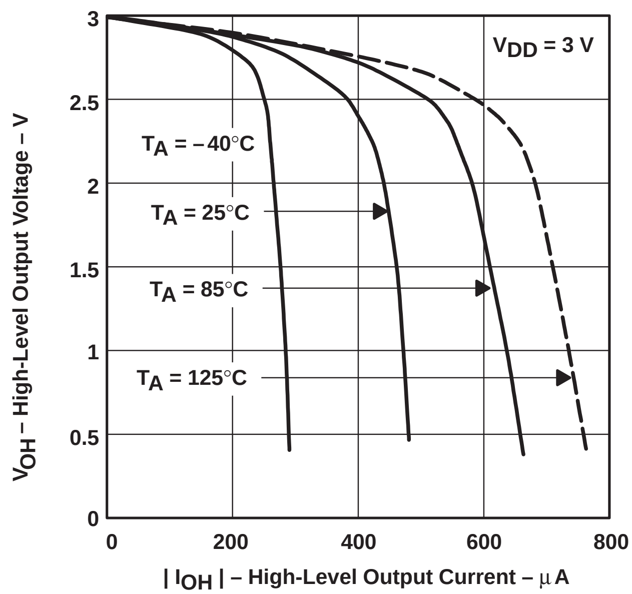



Figure 11

**LOW-LEVEL OUTPUT VOLTAGE‡ vs LOW-LEVEL OUTPUT CURRENT**

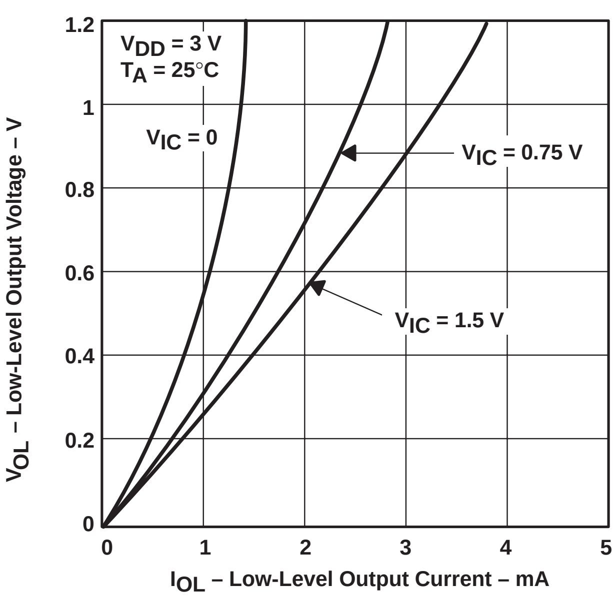



Figure 12

**LOW-LEVEL OUTPUT VOLTAGE†‡ vs LOW-LEVEL OUTPUT CURRENT**

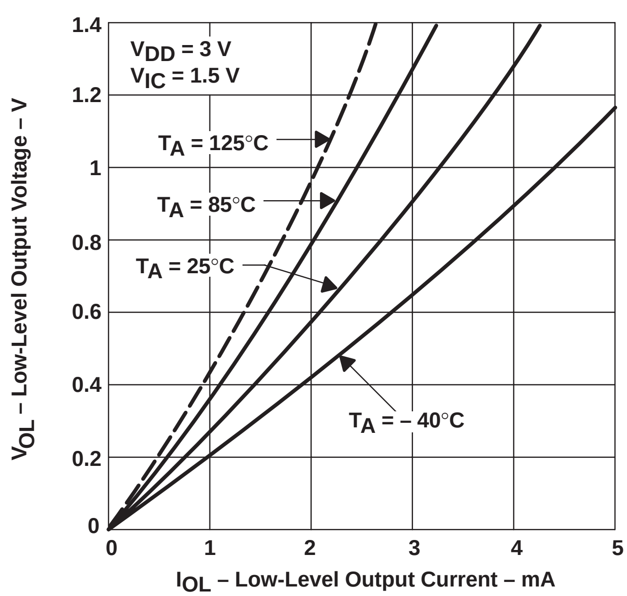



Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where $V_{DD}$ = 5 V, all loads are referenced to 2.5 V. For all curves where $V_{DD}$ = 3 V, all loads are referenced to 1.5 V.

## TYPICAL CHARACTERISTICS

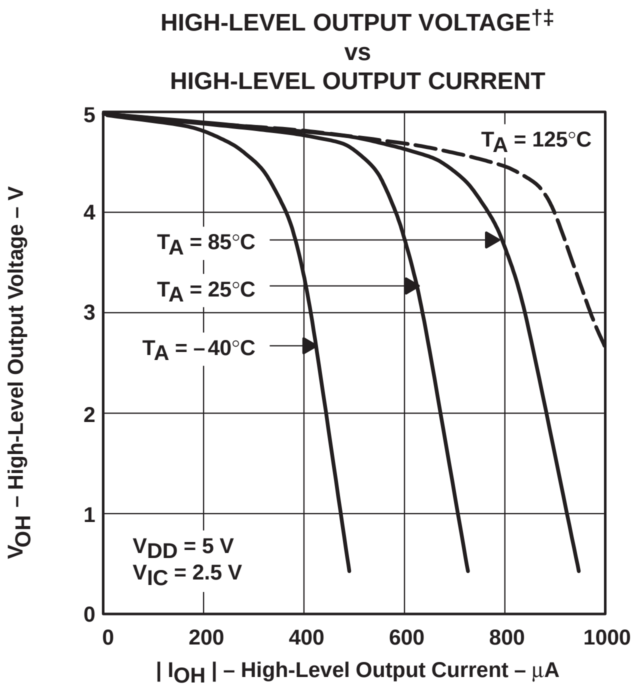



Figure 14

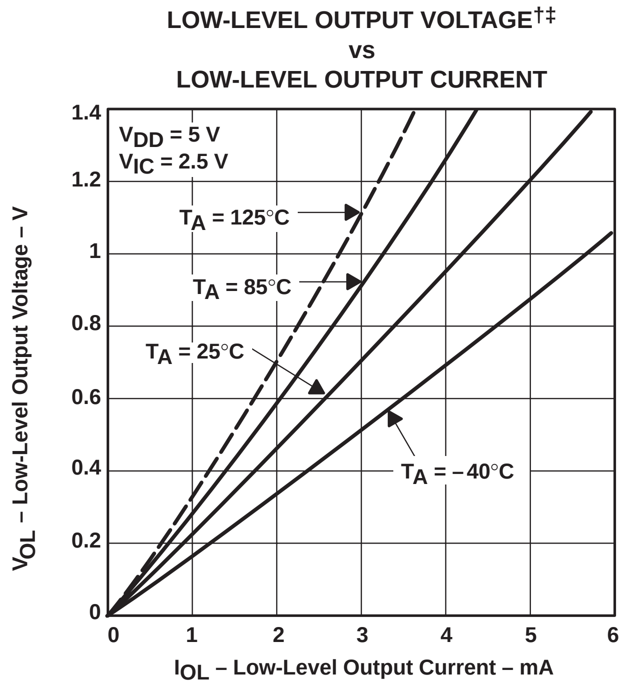



Figure 15

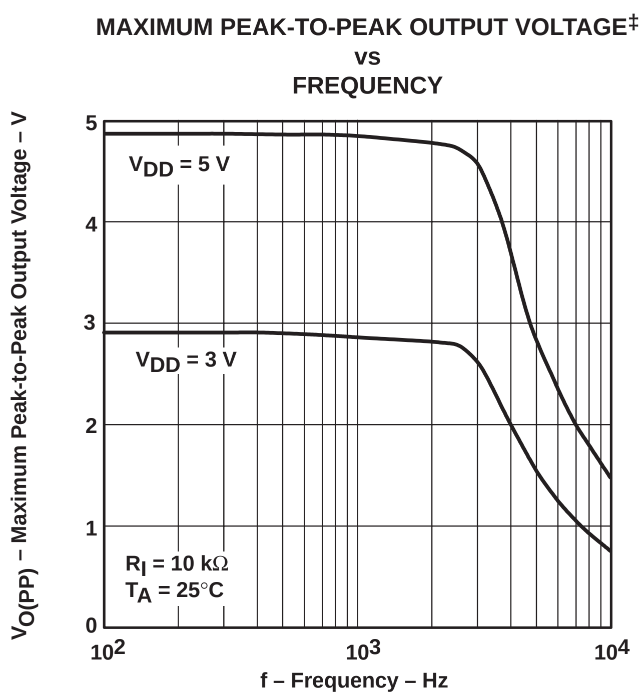



Figure 16

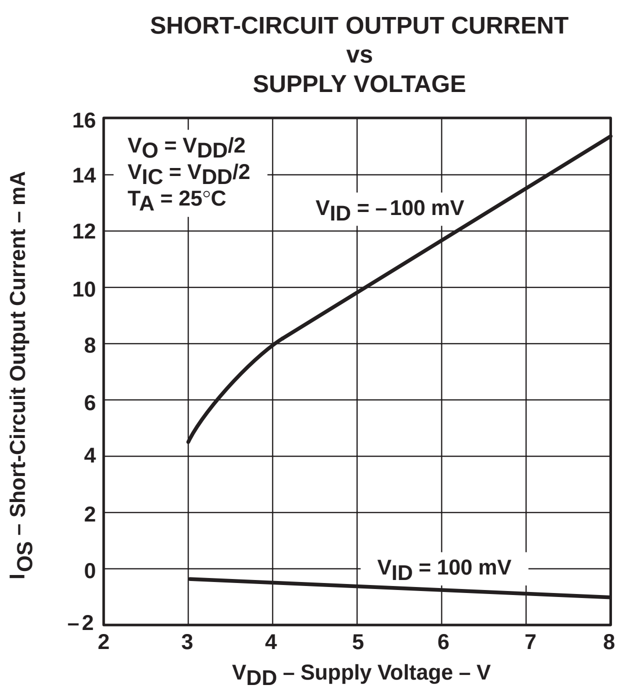



Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where $V_{DD}$ = 5 V, all loads are referenced to 2.5 V. For all curves where $V_{DD}$ = 3 V, all loads are referenced to 1.5 V.

## TYPICAL CHARACTERISTICS

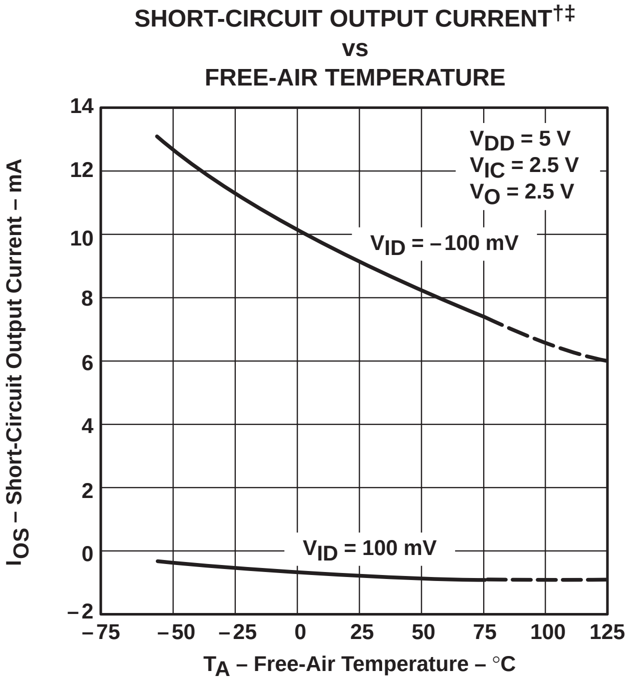



Figure 18

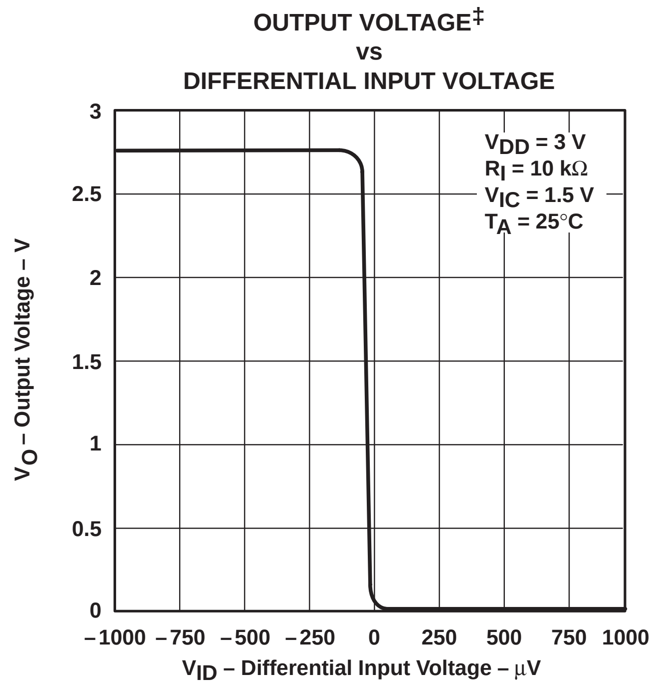



Figure 19

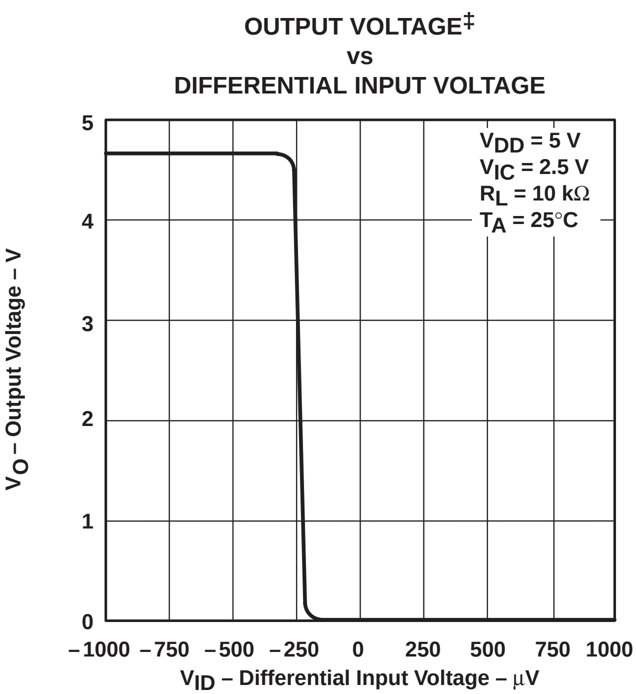



Figure 20

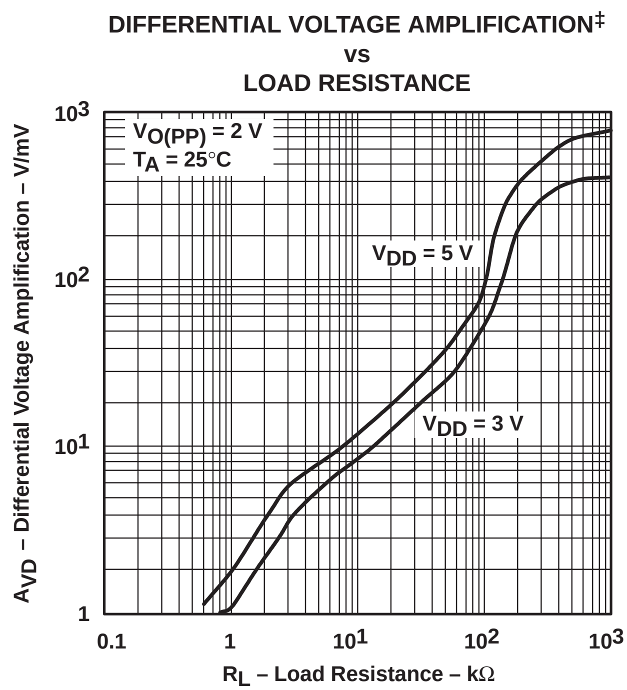



Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where $V_{DD}$ = 5 V, all loads are referenced to 2.5 V. For all curves where $V_{DD}$ = 3 V, all loads are referenced to 1.5 V.

## TYPICAL CHARACTERISTICS

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN†**
**vs**
**FREQUENCY**

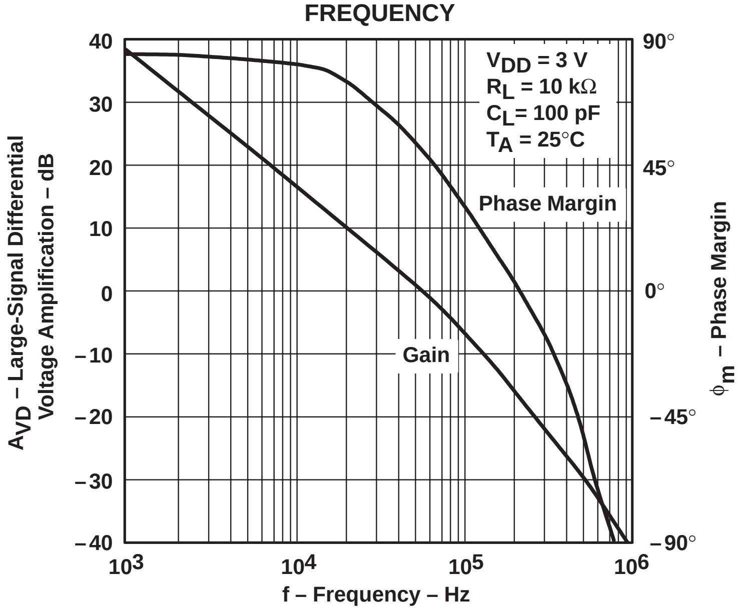



**Figure 22**

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN†**
**vs**
**FREQUENCY**

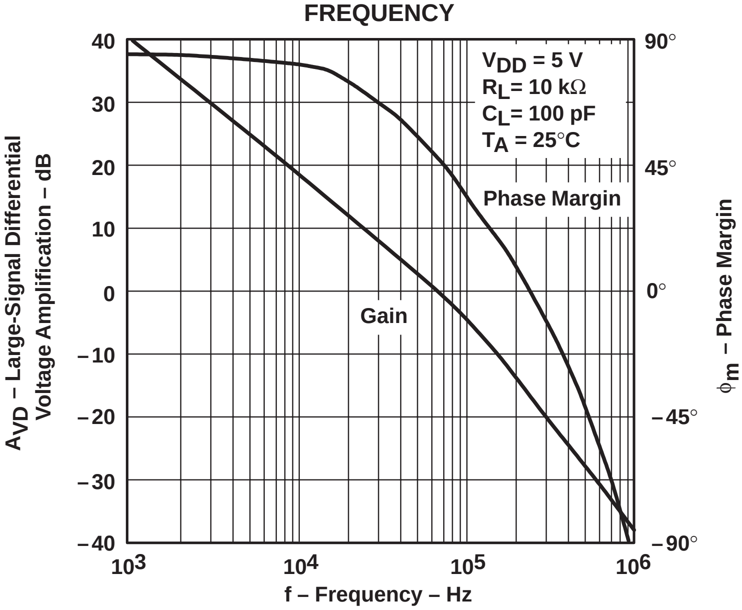



**Figure 23**

† For all curves where $V_{DD}$ = 5 V, all loads are referenced to 2.5 V. For all curves where $V_{DD}$ = 3 V, all loads are referenced to 1.5 V.

## TYPICAL CHARACTERISTICS

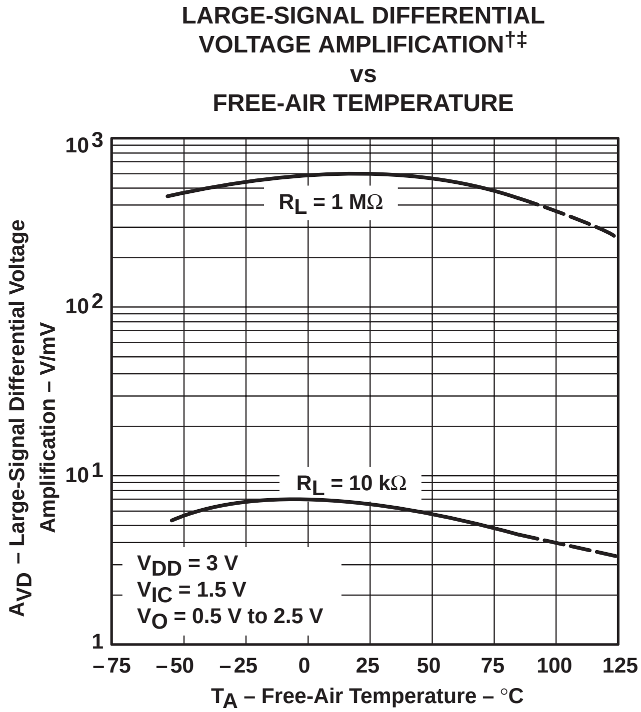



Figure 24

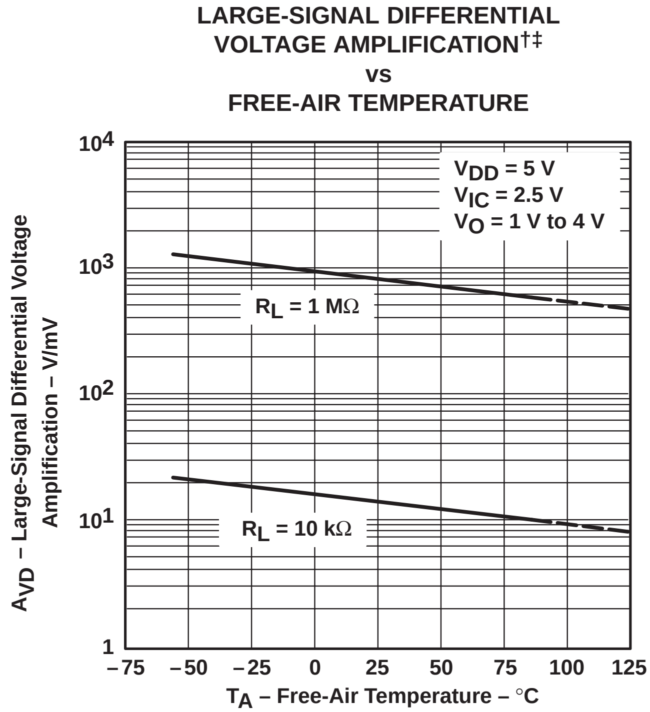



Figure 25

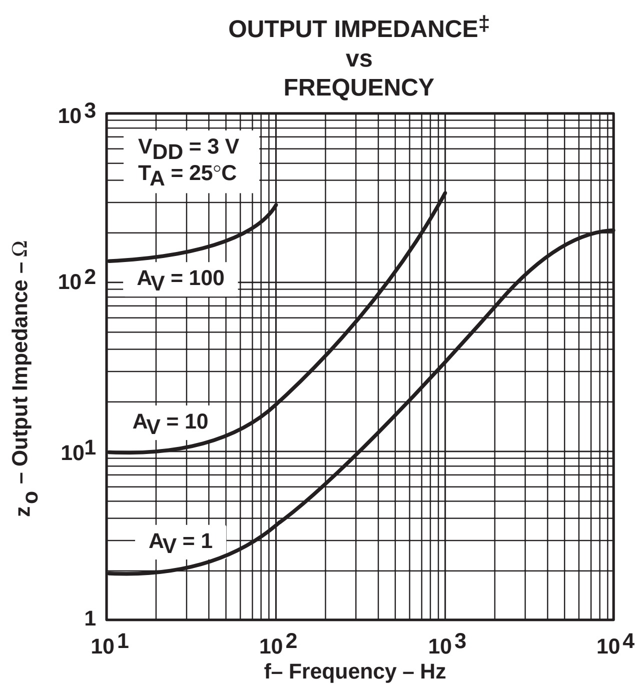



Figure 26

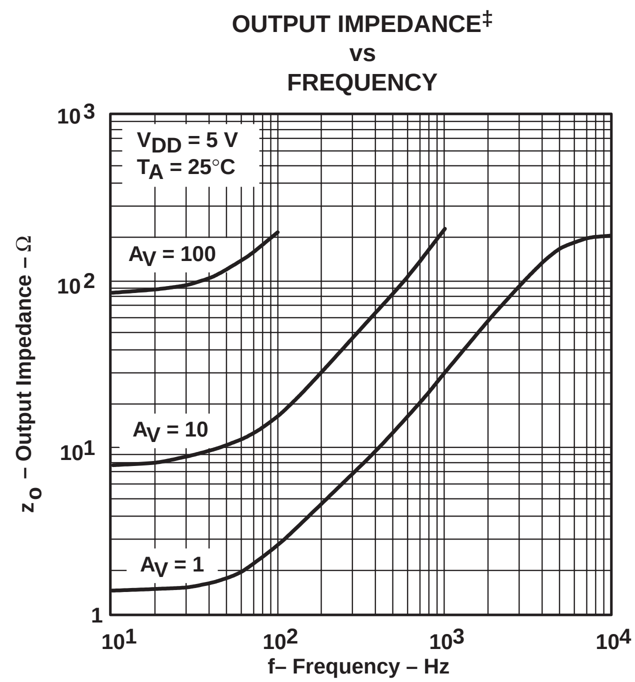



Figure 27

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where $V_{DD}$ = 5 V, all loads are referenced to 2.5 V. For all curves where $V_{DD}$ = 3 V, all loads are referenced to 1.5 V.

## TYPICAL CHARACTERISTICS

**COMMON-MODE REJECTION RATIO† vs FREQUENCY**

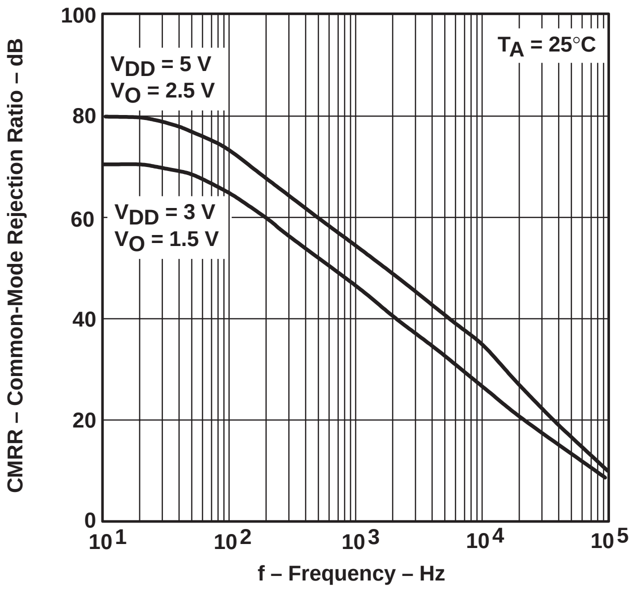



Figure 28

**COMMON-MODE REJECTION RATIO†‡ vs FREE-AIR TEMPERATURE**

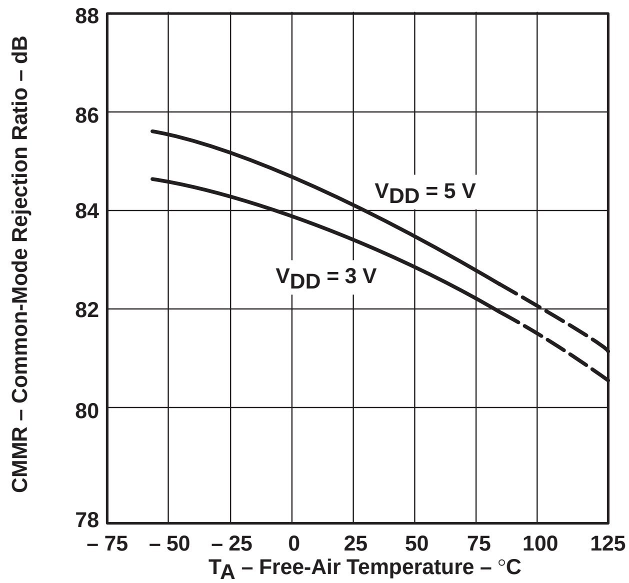



Figure 29

**SUPPLY-VOLTAGE REJECTION RATIO† vs FREQUENCY**

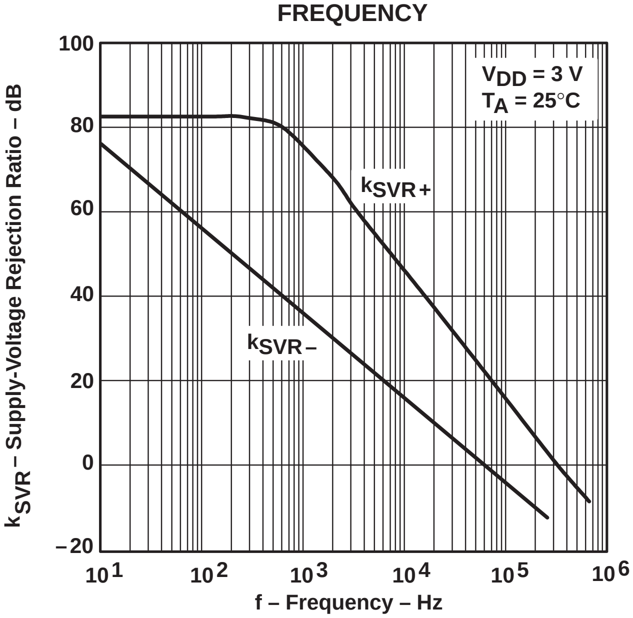



Figure 30

**SUPPLY-VOLTAGE REJECTION RATIO† vs FREQUENCY**

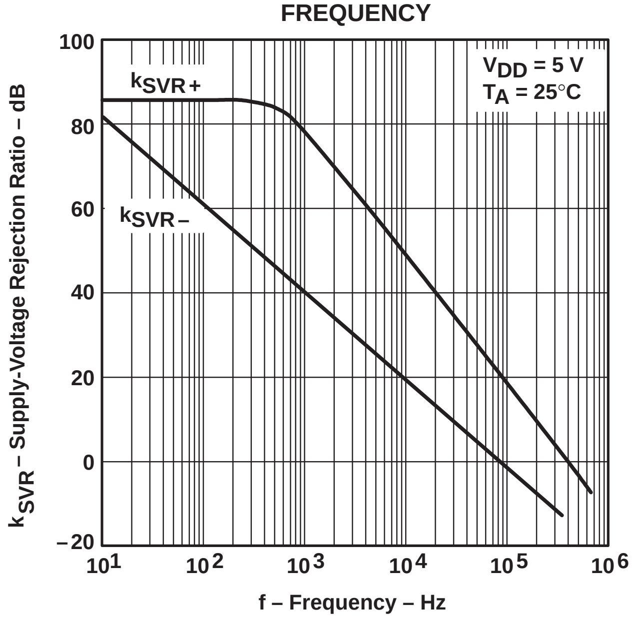



Figure 31

† For all curves where $V_{DD}$ = 5 V, all loads are referenced to 2.5 V. For all curves where $V_{DD}$ = 3 V, all loads are referenced to 1.5 V.
‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

## TYPICAL CHARACTERISTICS

**SUPPLY-VOLTAGE REJECTION RATIO†**
**vs**
**FREE-AIR TEMPERATURE**

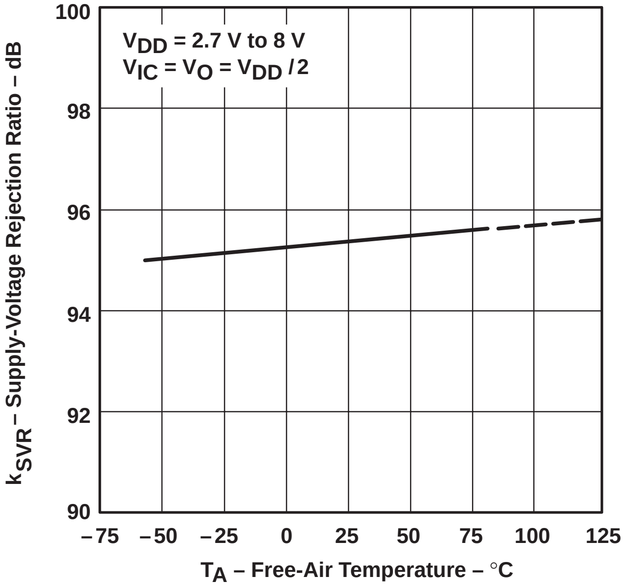



**Figure 32**

**SUPPLY CURRENT†**
**vs**
**SUPPLY VOLTAGE**

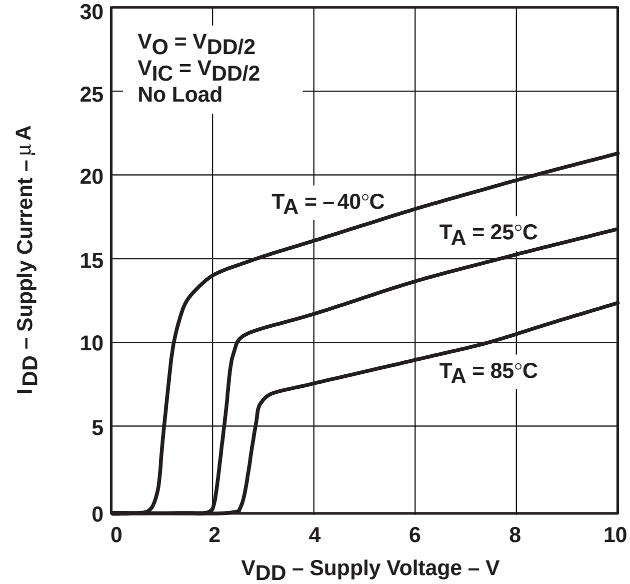



**Figure 33**

**SLEW RATE‡**
**vs**
**LOAD CAPACITANCE**

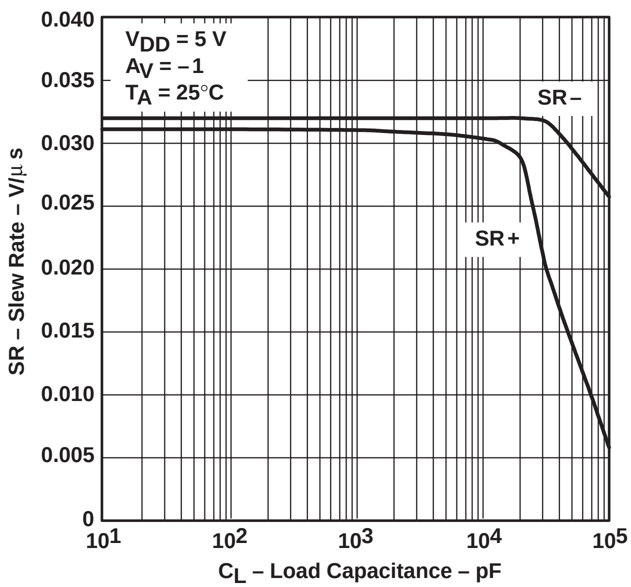



**Figure 34**

**SLEW RATE†‡**
**vs**
**FREE-AIR TEMPERATURE**

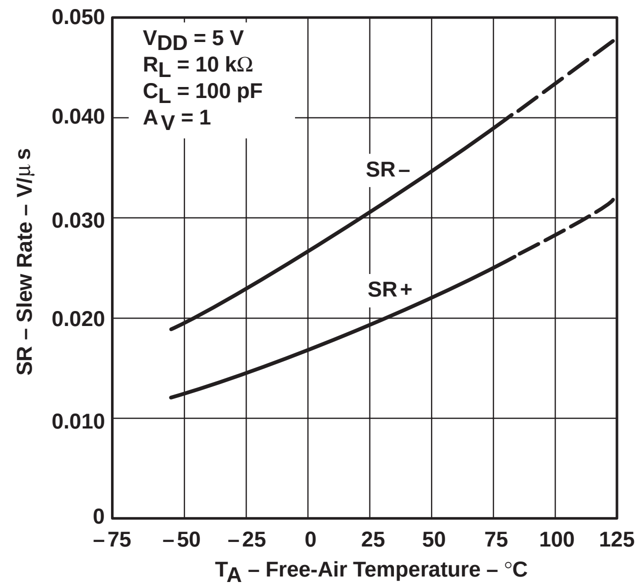



**Figure 35**

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where $V_{DD}$ = 5 V, all loads are referenced to 2.5 V. For all curves where $V_{DD}$ = 3 V, all loads are referenced to 1.5 V.

## TYPICAL CHARACTERISTICS

INVERTING LARGE-SIGNAL PULSE RESPONSE†

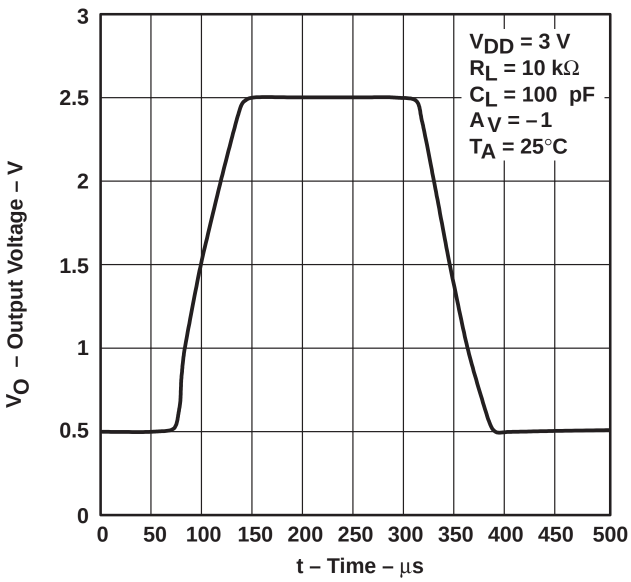



Figure 36

INVERTING LARGE-SIGNAL PULSE RESPONSE†

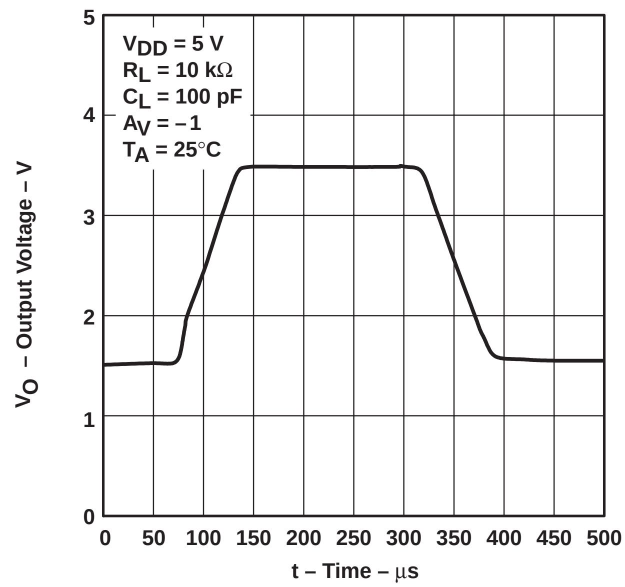



Figure 37

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

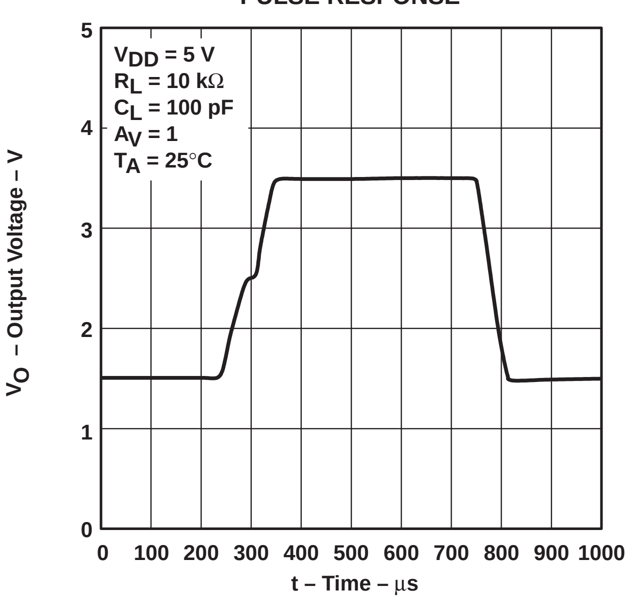



Figure 38

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

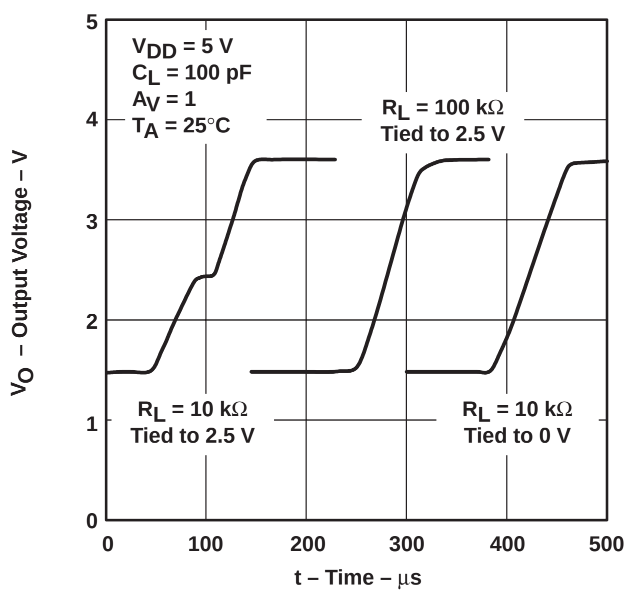



Figure 39

† For all curves where $V_{DD}$ = 5 V, all loads are referenced to 2.5 V. For all curves where $V_{DD}$ = 3 V, all loads are referenced to 1.5 V.

## TYPICAL CHARACTERISTICS

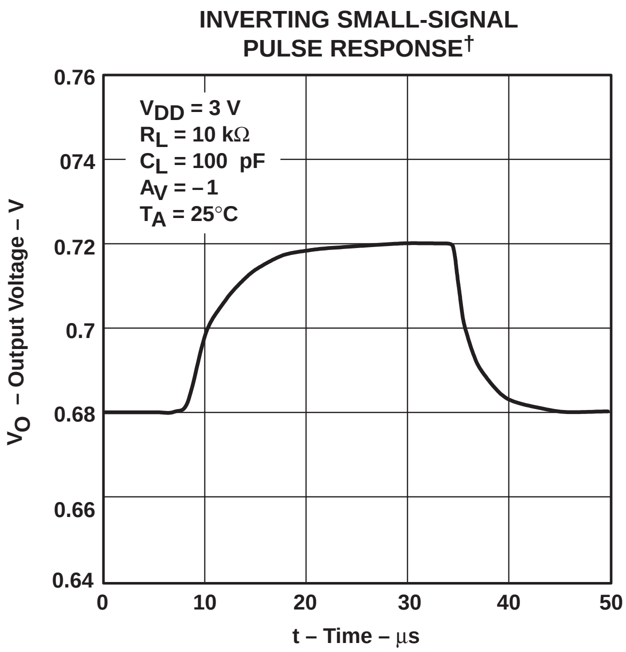



Figure 40

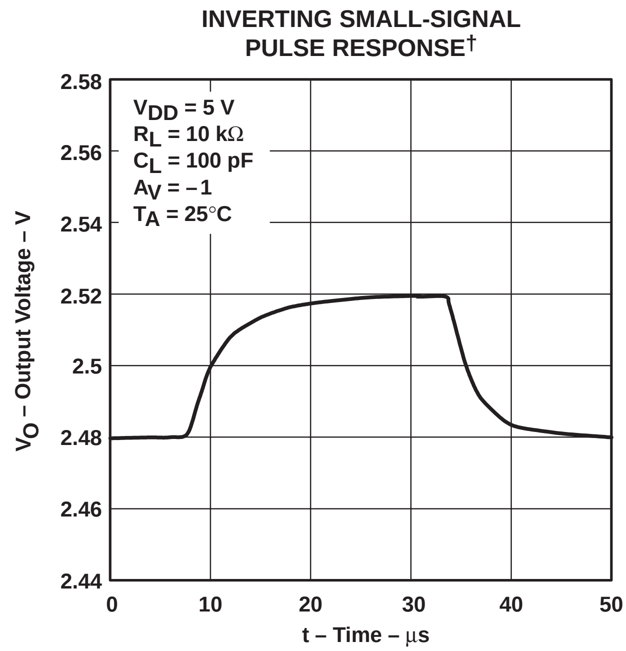



Figure 41

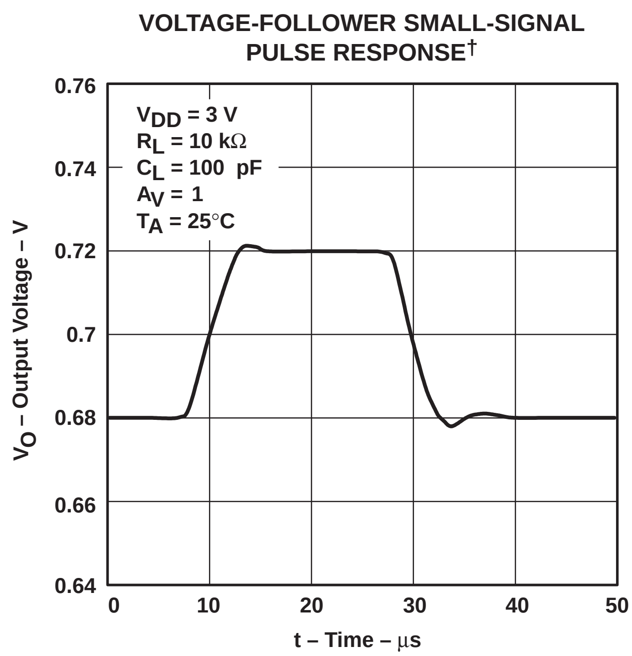



Figure 42

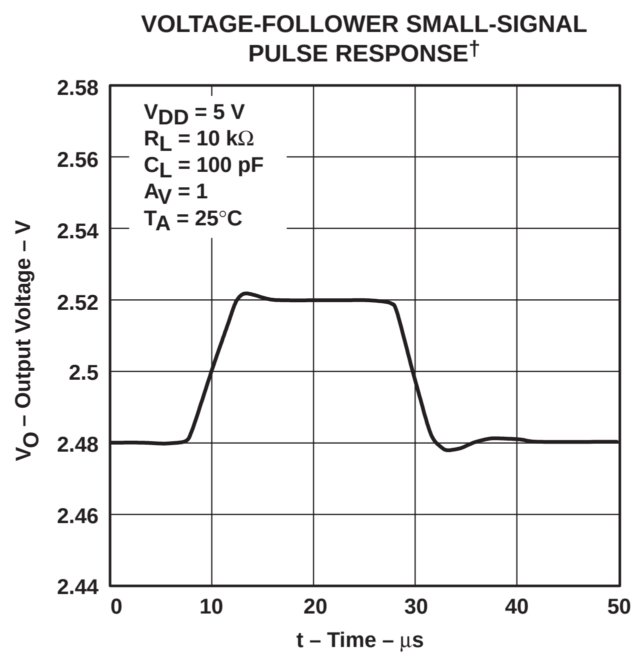



Figure 43

† For all curves where $V_{DD}$ = 5 V, all loads are referenced to 2.5 V. For all curves where $V_{DD}$ = 3 V, all loads are referenced to 1.5 V.

## TYPICAL CHARACTERISTICS

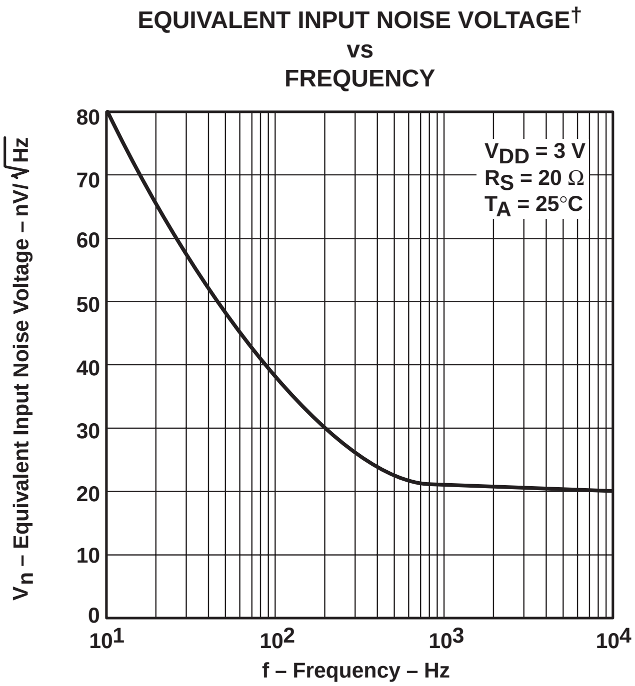



**Figure 44**

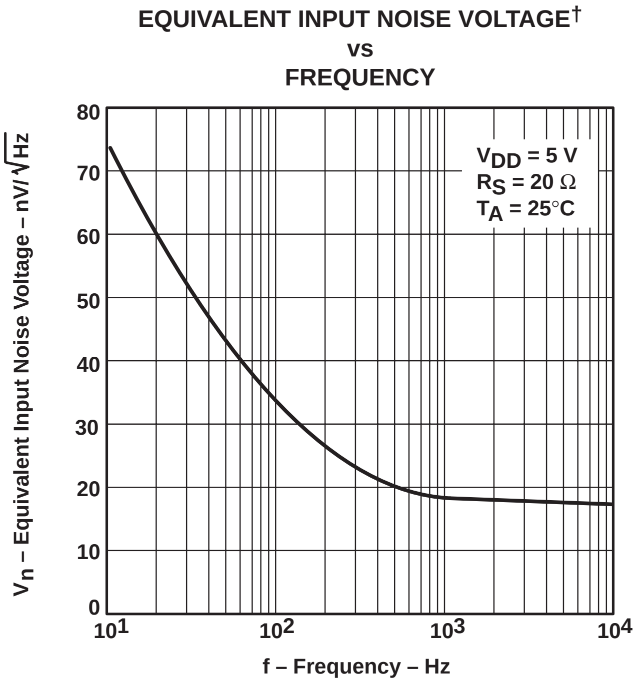



**Figure 45**

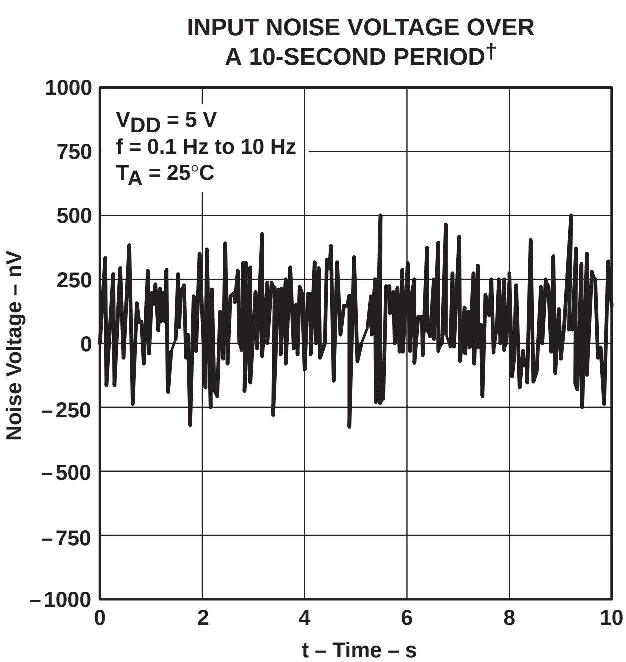



**Figure 46**

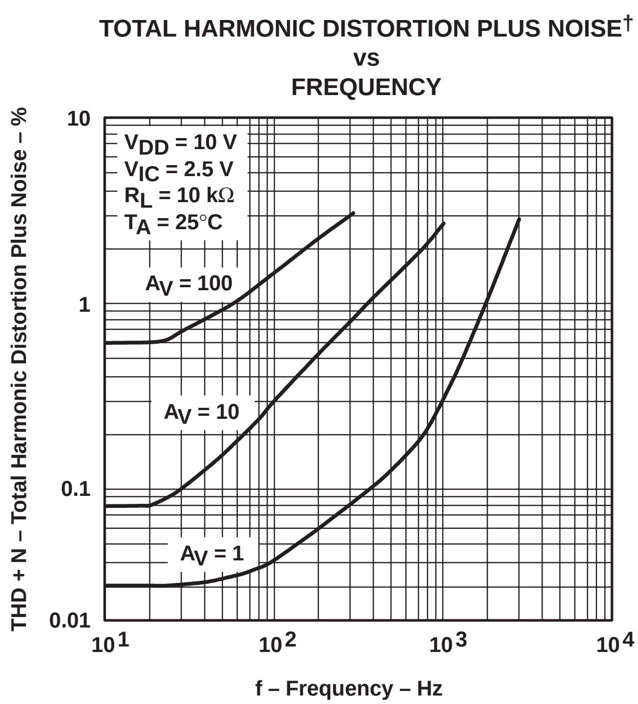



**Figure 47**

† For all curves where $V_{DD}$ = 5 V, all loads are referenced to 2.5 V. For all curves where $V_{DD}$ = 3 V, all loads are referenced to 1.5 V.

## TYPICAL CHARACTERISTICS

**GAIN-BANDWIDTH PRODUCT†‡ vs FREE-AIR TEMPERATURE**

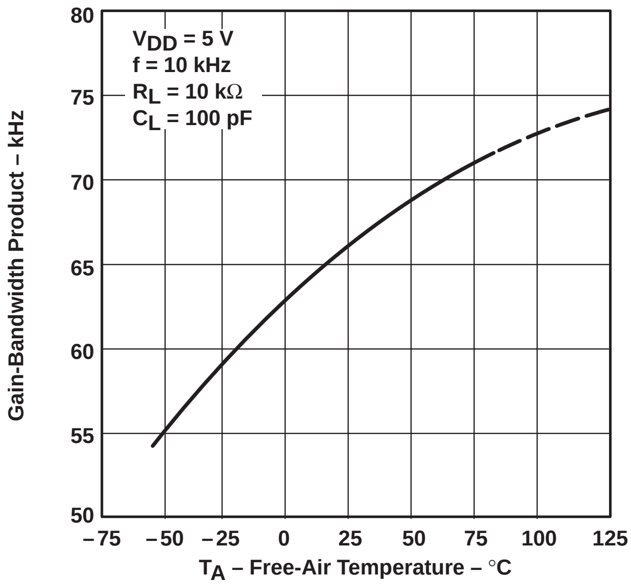



**Figure 48**

**GAIN-BANDWIDTH PRODUCT vs SUPPLY VOLTAGE**

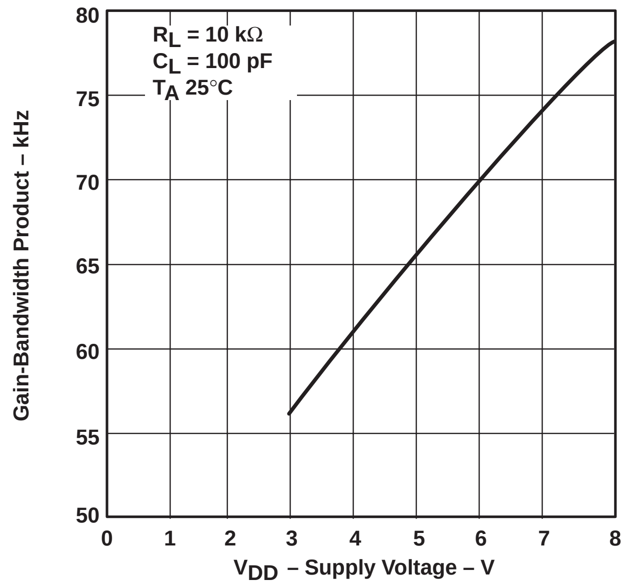



**Figure 49**

**PHASE MARGIN vs LOAD CAPACITANCE**

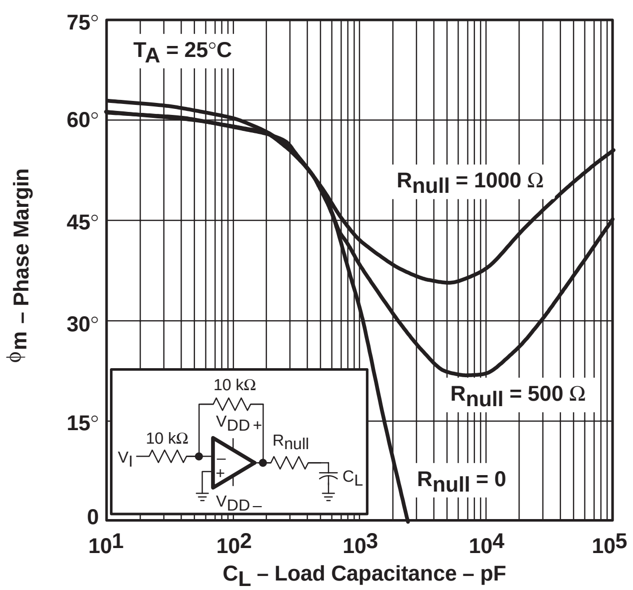



**Figure 50**

**GAIN MARGIN vs LOAD CAPACITANCE**

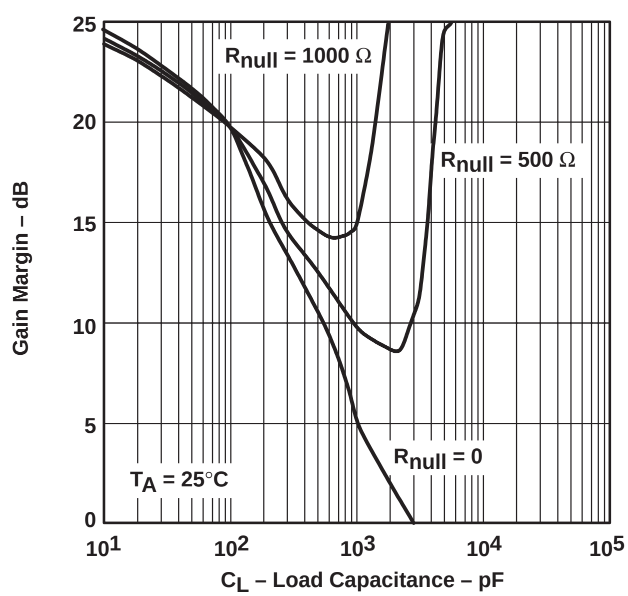



**Figure 51**

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where $V_{DD}$ = 5 V, all loads are referenced to 2.5 V. For all curves where $V_{DD}$ = 3 V, all loads are referenced to 1.5 V.

## TYPICAL CHARACTERISTICS

**UNITY-GAIN BANDWIDTH vs LOAD CAPACITANCE**

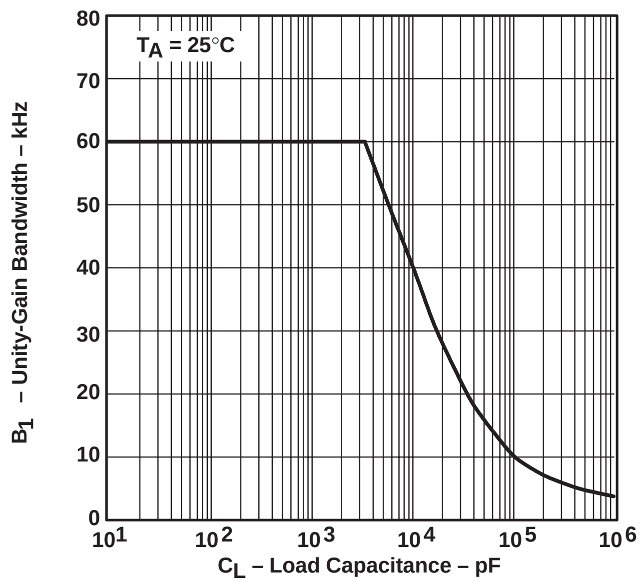



**Figure 52**

## APPLICATION INFORMATION

### driving large capacitive loads

The TLV2711 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 50 and Figure 51 illustrate its ability to drive loads up to 600 pF while maintaining good gain and phase margins ($R_{null}$ = 0).

A smaller series resistor ($R_{null}$) at the output of the device (see Figure 53) improves the gain and phase margins when driving large capacitive loads. Figure 50 and Figure 51 show the effects of adding series resistances of 500 Ω and 1000 Ω. The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation 1 can be used.

$$\Delta\phi_{m1} = \tan^{-1}\left(2 \times \pi \times UGBW \times R_{null} \times C_L\right) \quad (1)$$

Where :

$\Delta\phi_{m1}$ = Improvement in phase margin
UGBW = Unity-gain bandwidth frequency
$R_{null}$ = Output series resistance
$C_L$ = : Load capacitance

## APPLICATION INFORMATION

### driving large capacitive loads (continued)

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 52). To use equation 1, UGBW must be approximated from Figure 52.

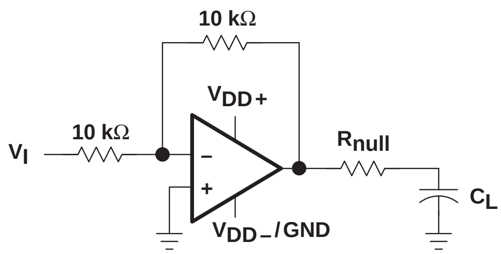



**Figure 53. Series-Resistance Circuit**

### driving heavy dc loads

The TLV2711 is designed to provide better sinking and sourcing output currents than earlier CMOS rail-to-rail output devices. This device is specified to sink 500 µA and source 250 µA at $V_{DD}$ = 3 V and $V_{DD}$ = 5 V at a maximum quiescent $I_{DD}$ of 25 µA. This provides a greater than 90% power efficiency.

When driving heavy dc loads, such as 10 kΩ, the positive edge under slewing conditions can experience some distortion. This condition can be seen in Figure 38. This condition is affected by three factors.

- Where the load is referenced. When the load is referenced to either rail, this condition does not occur. The distortion occurs only when the output signal swings through the point where the load is referenced. Figure 39 illustrates two 10-kΩ load conditions. The first load condition shows the distortion seen for a 10-kΩ load tied to 2.5 V. The third load condition shows no distortion for a 10-kΩ load tied to 0 V.
- Load resistance. As the load resistance increases, the distortion seen on the output decreases. Figure 39 illustrates the difference seen on the output for a 10-kΩ load and a 100-kΩ load with both tied to 2.5 V.
- Input signal edge rate. Faster input edge rates for a step input result in more distortion than with slower input edge rates.

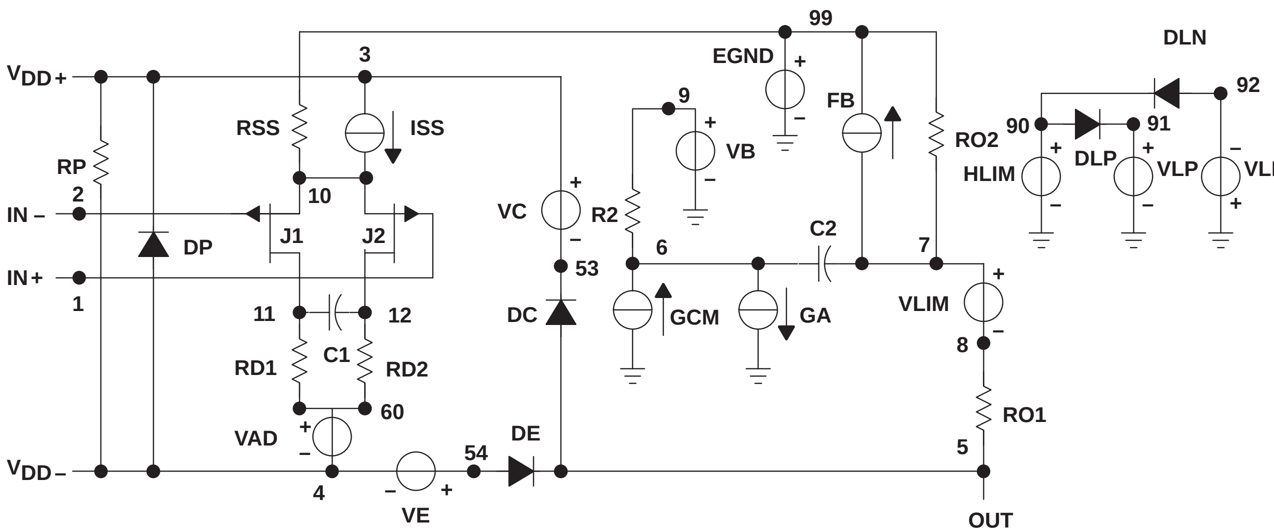
## APPLICATION INFORMATION

### macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 6) and subcircuit in Figure 54 are generated using the TLV2711 typical electrical and operating characteristics at $T_A$ = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 6: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).



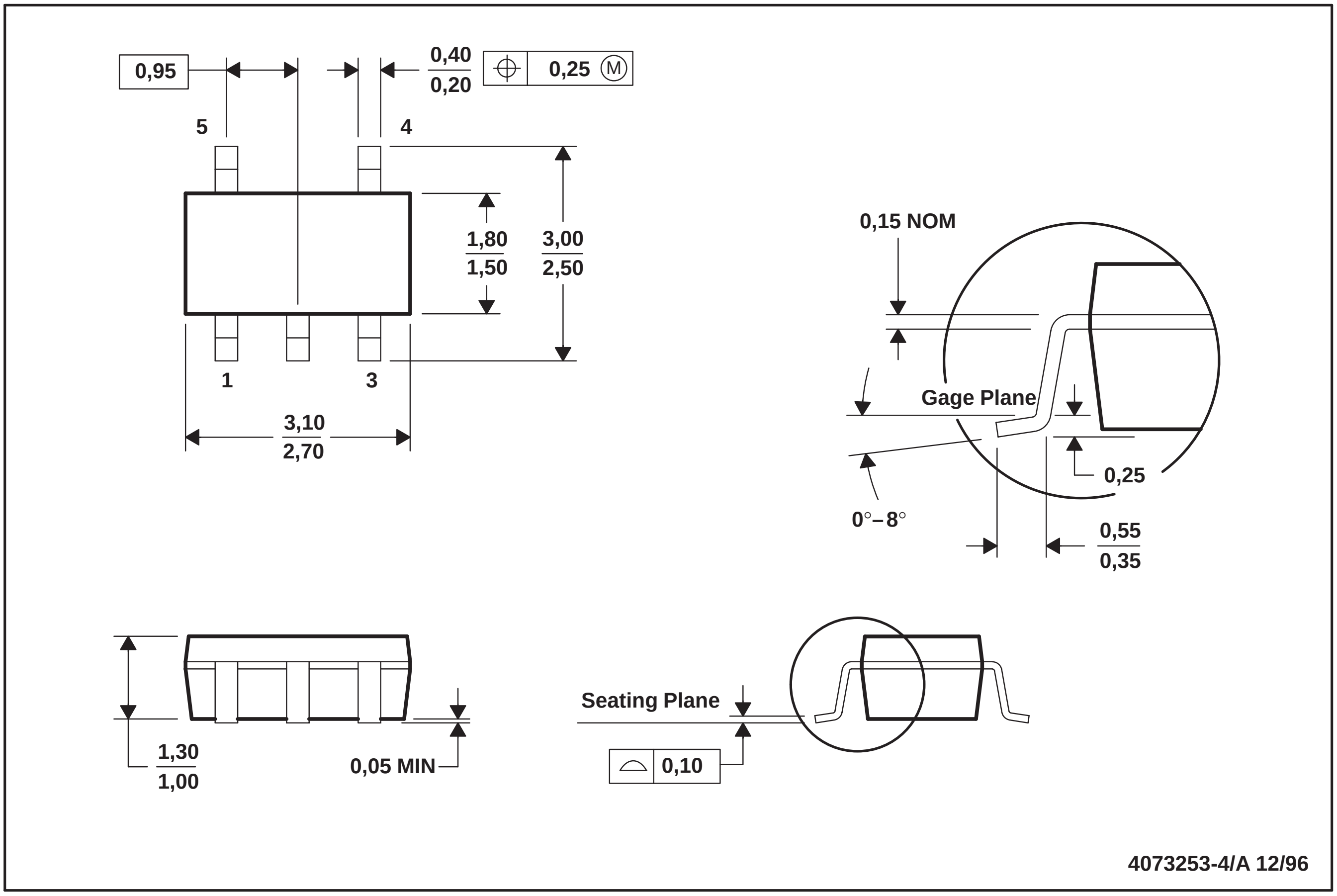

```
.SUBCKT TLV2711 1 2 3 4 5
        C1      11   12   8.86E–12
        C2      6    7    50.00E–12
        DC      5    53   DX
        DE      54   5    DX
        DLP     90   91   DX
        DLN     92   90   DX
        DP      4    3    DX
        EGND    99   0    POLY (2) (3,0) (4,0) 0 .5 .5
        FB      7    99   POLY (5) VB VC VE VLP
        + VLN 0 4.29E6 –6E6 6E6 6E6 –6E6
        GA      6    0    11   12 9.425E–6
        GCM     0    6    10   99 1320.2E–12
        ISS     3    10   DC 1.250E–6
        HLIM    90   0    VLIM 1K
        J1      11   2    10 JX
        J2      12   1    10 JX
        R2      6    9    100.0E3
RD1     60   11   106.1E3
RD2     60   12   106.1E3
R01     8    5    50
R02     7    99   150
RP      3    4    419.2E3
RSS     10   99   160.0E6
VAD     60   4    –.5
VB      9    0    DC 0
VC      3    53   DC .55
VE      54   4    DC .55
VLIM    7    8    DC 0
VLP     91   0    DC 0.1
VLN     0    92   DC 2.6
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=500.0E–15 BETA=166E–6
+ VTO=–.004)
.ENDS
```

**Figure 54. Boyle Macromodel and Subcircuit**

*PSpice* and *Parts* are trademark of MicroSim Corporation.

## MECHANICAL INFORMATION

**DBV (R-PDSO-G5)** **PLASTIC SMALL-OUTLINE PACKAGE**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| TLV2711CDBV | OBSOLETE | SOT-23 | DBV | 5 | | TBD | Call TI | Call TI |
| TLV2711CDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLV2711CDBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLV2711CDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLV2711CDBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLV2711IDBV | OBSOLETE | SOT-23 | DBV | 5 | | TBD | Call TI | Call TI |
| TLV2711IDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLV2711IDBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLV2711IDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLV2711IDBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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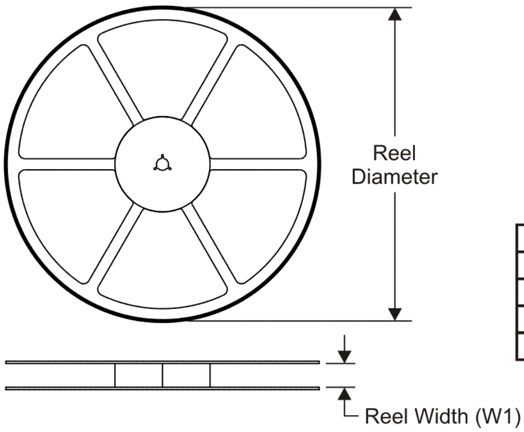
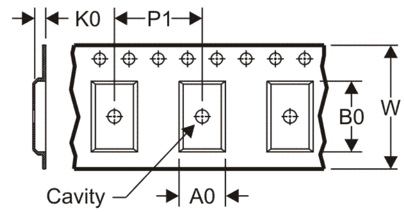
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

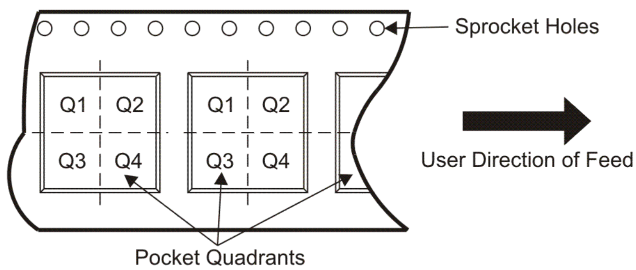



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

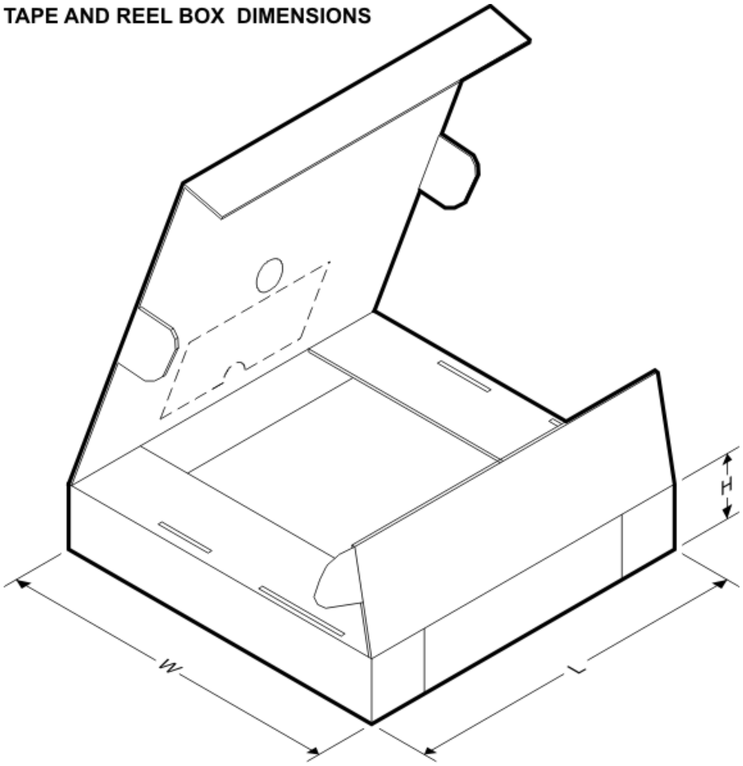
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV2711CDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV2711CDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV2711IDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV2711IDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

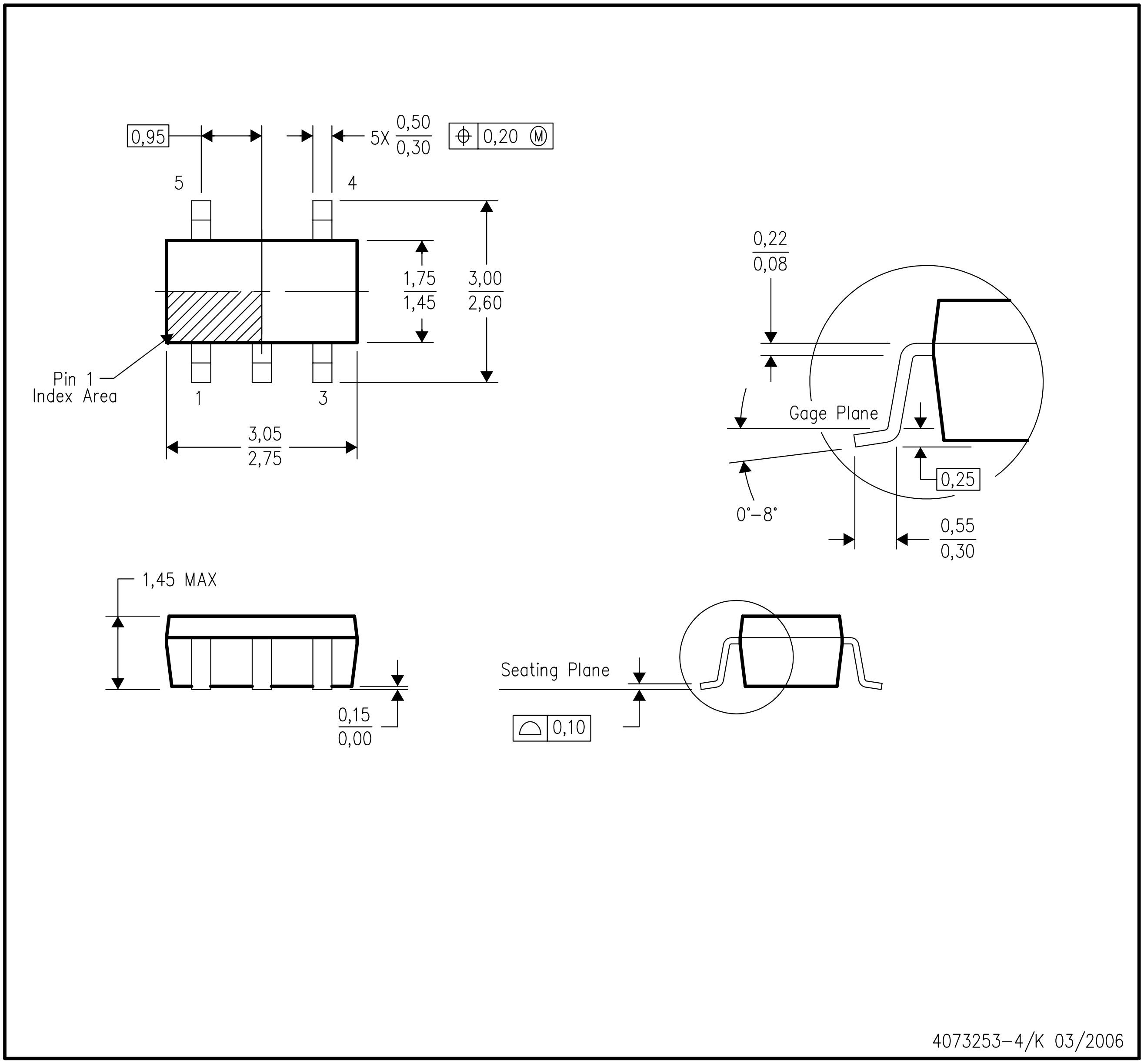
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV2711CDBVR | SOT-23 | DBV | 5 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV2711CDBVT | SOT-23 | DBV | 5 | 250 | 182.0 | 182.0 | 20.0 |
| TLV2711IDBVR | SOT-23 | DBV | 5 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV2711IDBVT | SOT-23 | DBV | 5 | 250 | 182.0 | 182.0 | 20.0 |

DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE




NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.